PRELIMINARY
APPLICATION NOTE

TJA1041
CAN High-Speed Transceiver

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Philips
Semiconductors

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Abstract

The TJA1041 is an advanced CAN High-Speed Transceiver for use in automotive and general industrial applications. CAN (Controller Area Network) has become the de-facto standard protocol for serial in-vehicle bus communication, particularly for Powertrain and Body Multiplexing.

The TJA1041 features the low power management known from the Fault Tolerant CAN Transceiver TJA1054. Accordingly, the TJA1041 is predestined for Electronic Control Units (ECUs), which are continuously supplied by battery regardless of ignition key. Furthermore, the TJA1041 offers enhanced diagnosis features. Local failures, like short circuits between pins, as well as bus wiring failures are detected and reported to the host microcontroller.

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PRELIMINARY APPLICATION NOTE

TJA1041 CAN High-Speed Transceiver

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Summary

This application note provides information how to use the TJA1041 within automotive and industrial applications. It in detail describes the functional behaviour and how to exploit the outstanding performance of the TJA1041. Main focus is on new features like low power management, diagnosis of bus wiring failures and local failures (pin short-circuits) and common mode stabilization.

Interoperability with the CAN High-Speed Transceiver PCA82C250/251, TJA1050 and TJA1040 from Philips Semiconductors is also considered.

Revision History

Version	Remarks
19.04.2001	Initial Version
25.09.2002	Updated Version - New chapter “Target Applications for the TJA1041” - Update of chapter “Hardware Application of the TJA1041” - New chapter “Flag Signalling” - Previous chapter “Diagnosis” split into chapter “Bus Failure Diagnosis” and “Local Failure Diagnosis” - New chapter “Under-voltage Detection” - Update of chapter “Interoperability”

Contents

1. INTRODUCTION

The CAN High-Speed Transceiver TJA1041 [1] from Philips Semiconductors provides the physical link between the protocol controller and the physical transmission medium according to ISO11898 [2] and SAE J2284 [3]. It has been developed to address mainly those control applications within automotive electronics, which remain supplied by the battery during the whole lifetime of the vehicle. Focusing on these applications the TJA1041 offers a low power management similar to that of the Fault-tolerant CAN Transceiver TJA1054 [4]. According to this concept one or more external voltage regulators within the Electronic Control Unit (ECU) are controlled autonomously by the transceiver. This concept allows a TJA1041 entering Sleep Mode to switch these voltage regulators off, disabling the Vcc supply of the transceiver and the host microcontroller.

The TJA1041 is available without packaging (naked die) as well as in SO14 package as shown in Figure 1-1. The upper part of the SO14 pinning is compatible to the SO8 pinning of other CAN High-Speed Transceivers from Philips Semiconductors like the PCA82C250 [5], PCA82C251 [6], TJA1050 [7] and TJA1040 [8].

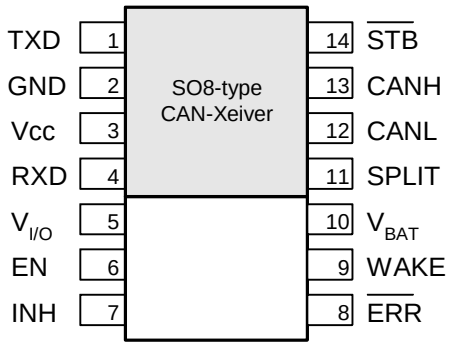


Figure 1-1: Pinning of the TJA1041

2. GENERAL APPLICATION OF CAN HIGH-SPEED

A general application of CAN High-Speed is illustrated in Figure 2-1. Here a linear bus topology is shown with the ECUs connected to the bus via stubs. Each bus end is terminated with 120Ω, resulting in the nominal 60Ω bus load according to ISO11898 [2]. Figure 2-1 shows the Split Termination concept, which is helpful in improving the EMC of CAN High-Speed bus systems [9]. The former single 120Ω termination resistor is split into two resistors of half value with the center tap connected to ground via the capacitor C_{spl}.

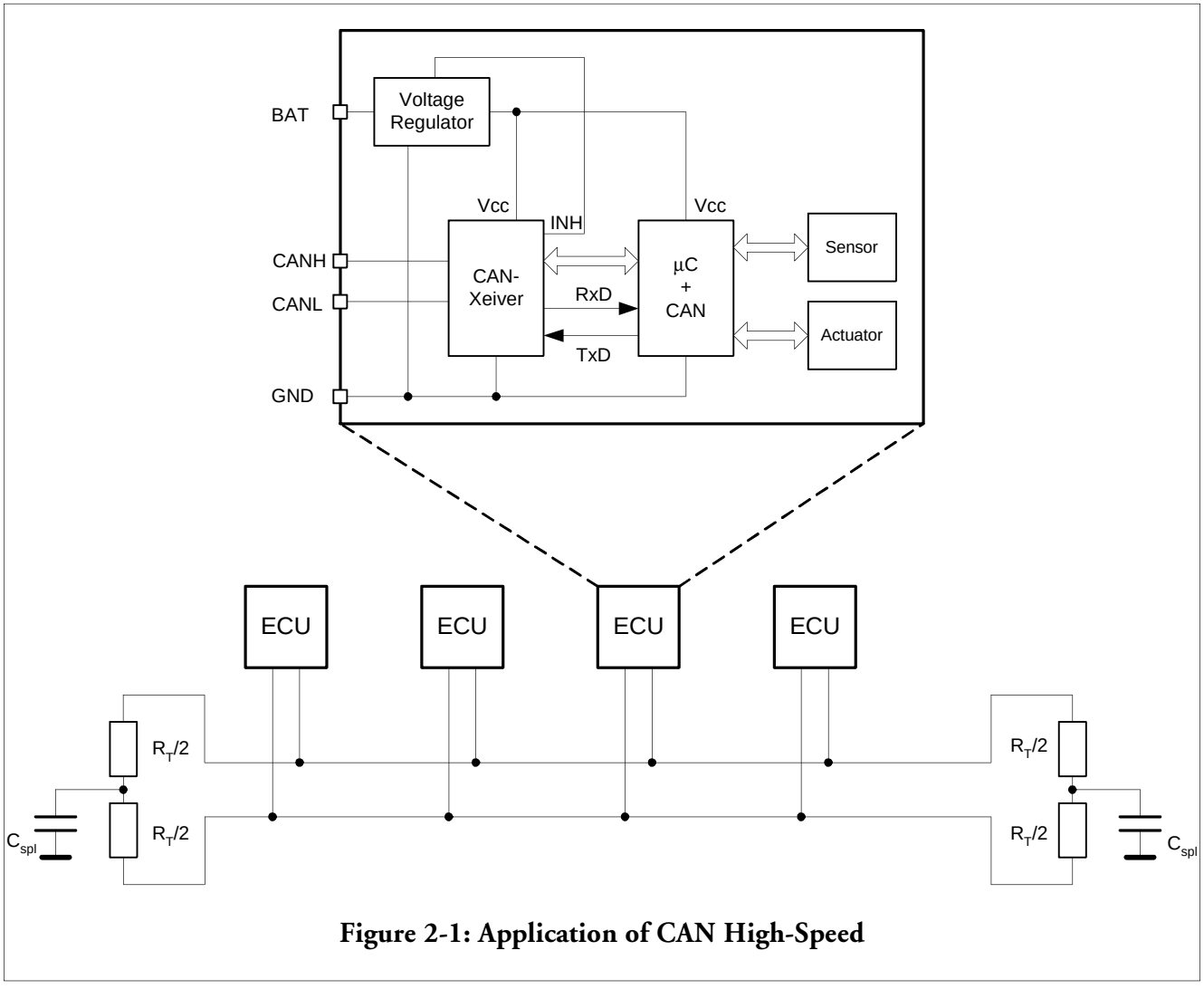


Figure 2-1: Application of CAN High-Speed

The block diagram in Figure 2-1 furthermore describes the structure of an ECU. Typically an ECU (CAN-node) consists of a standalone transceiver and a host microcontroller with integrated CAN-controller, which are supplied by a voltage regulator. While the CAN High-Speed Transceiver needs a +5V supply, new microcontroller products are increasingly using lower supply voltages. In this case a dedicated voltage regulator is necessary for the microcontroller. The protocol controller is connected to the transceiver via a serial data output line (TxD) and a serial data input line (RxD). The transceiver is attached to the bus lines via its two bus terminals CANH and CANL, which provide differential receive

and transmit capability. In case of the TJA1041 there is an additional INH signal line (indicated in Figure 2-1) controlling the voltage regulator. Giving the TJA1041 control over the voltage regulator(s) for Vcc and uC supply voltage allows for an extremely low ECU quiescent current.

The protocol controller outputs a serial transmit data stream to the TxD input of the transceiver. An internal pull-up function within the TJA1041 sets the TxD input to logic HIGH i.e. the bus output driver is passive in open circuit condition. In the so-called recessive state (see Figure 2-2) the CANH and CANL pins are biased to a voltage level of Vcc/2. In case a logic LOW-level is applied to TxD, this activates the bus output stage, thus generating a so-called dominant state on the bus line (Figure 2-2). The output driver CANH provides a source output from Vcc and the output driver CANL a sink output towards GND. This is illustrated in Figure 2-3 showing the block diagram of the TJA1041.

The bus stays in recessive state if no bus node transmits a dominant bit. If one or multiple bus nodes transmit a dominant bit, then the bus lines enter the dominant state thus overriding the recessive state (wired-AND characteristic).

The receiver converts the differential bus signal to a logic level signal, which is output at RxD. The serial receive data stream is provided to the bus protocol controller for decoding. The receiver comparator is always active i.e. it monitors the bus while the bus node is transmitting a message. This is required to support the non-destructive bit by bit arbitration scheme of CAN.

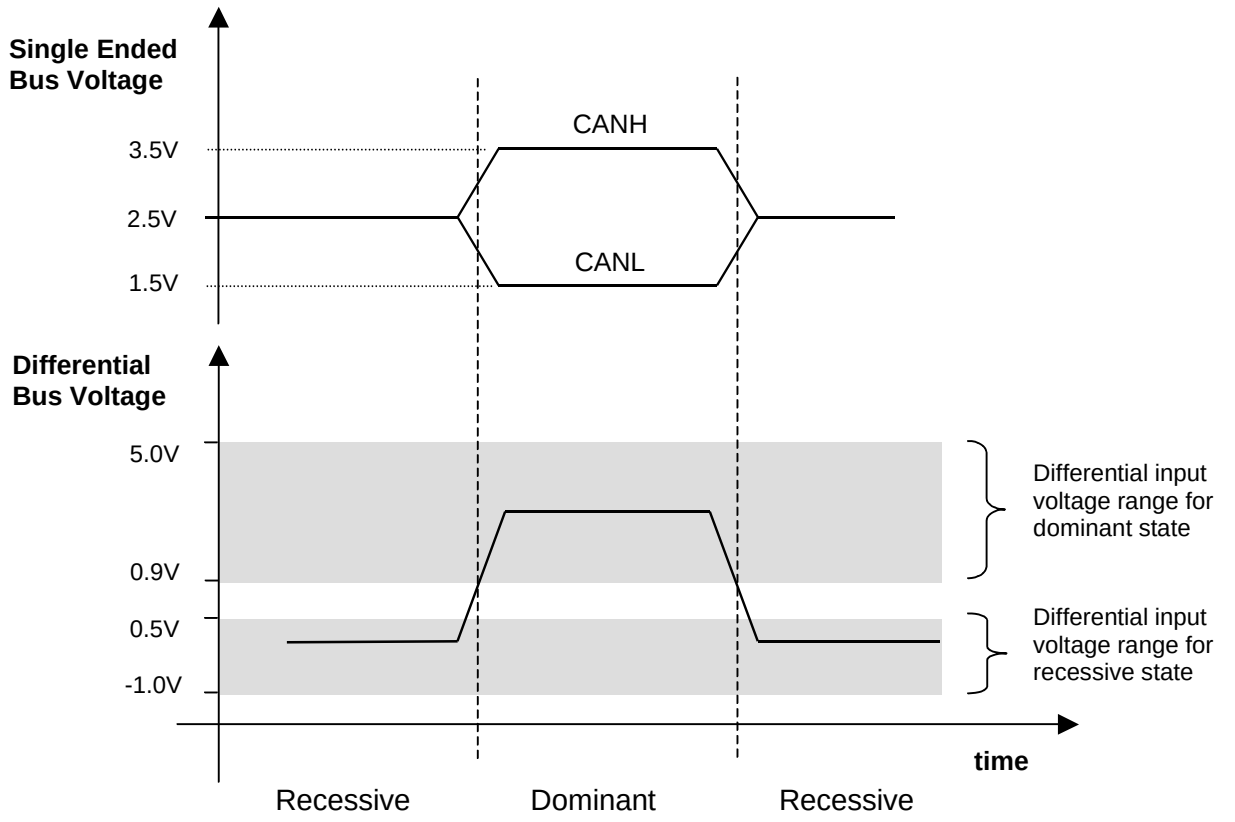


Figure 2-2: Nominal bus levels according to ISO11898

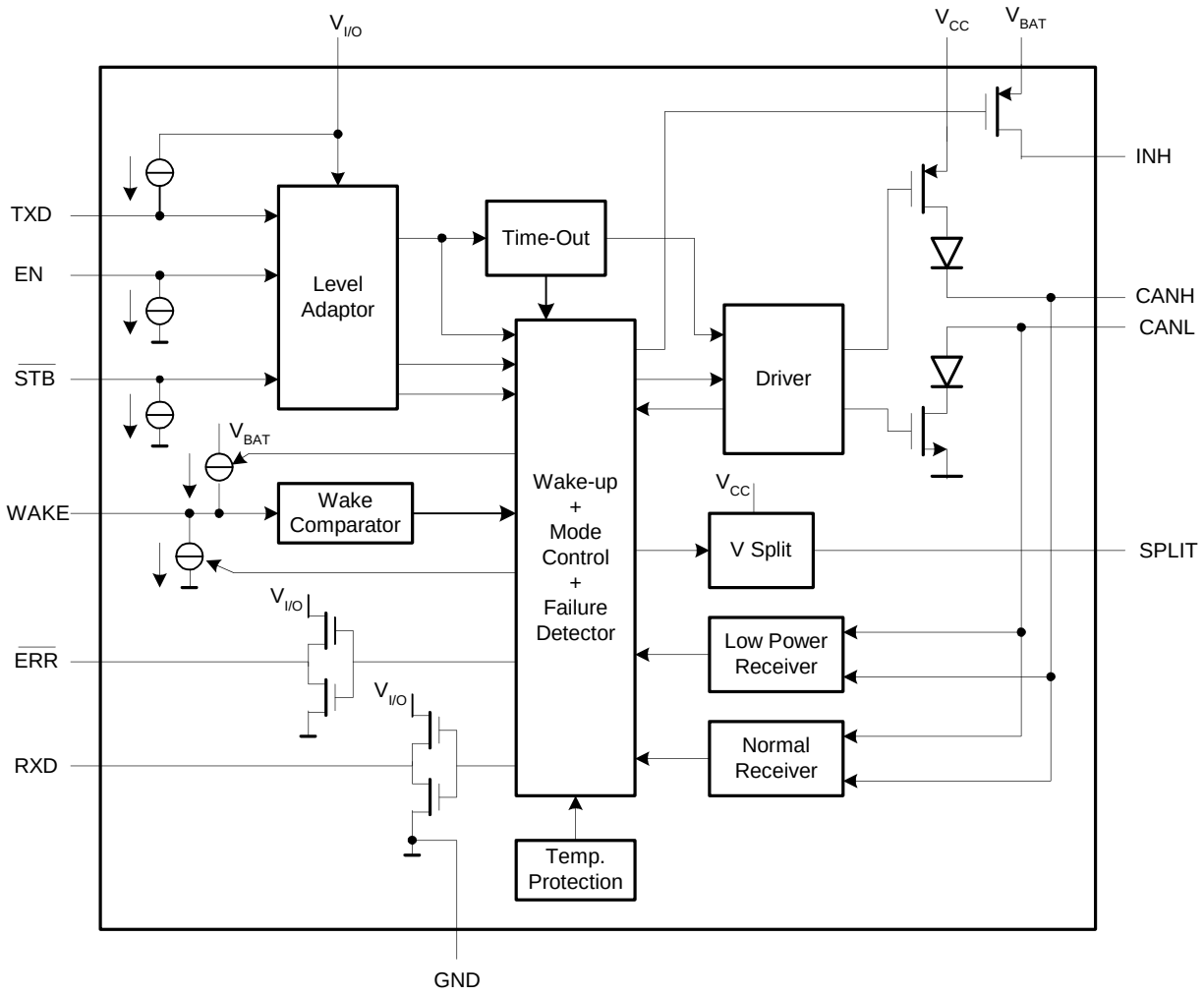


Figure 2-3: Block diagram of the TJA1041

3. TARGET APPLICATIONS FOR THE TJA1041

The High-Speed CAN Transceiver TJA1041 is the ideal choice for applications, which require a high data throughput (up to 1Mbit/s), bus diagnosis and enhanced low-power management. While the focus of the High-Speed CAN bus was mainly on powertrain applications, particularly the low-power management of the TJA1041 enables the High-Speed CAN bus also for other in-vehicle multiplexing tasks like body multiplexing and ITS data bus [10].

From ECU power management point of view, typically three different applications can be distinguished as illustrated in Figure 3-1.

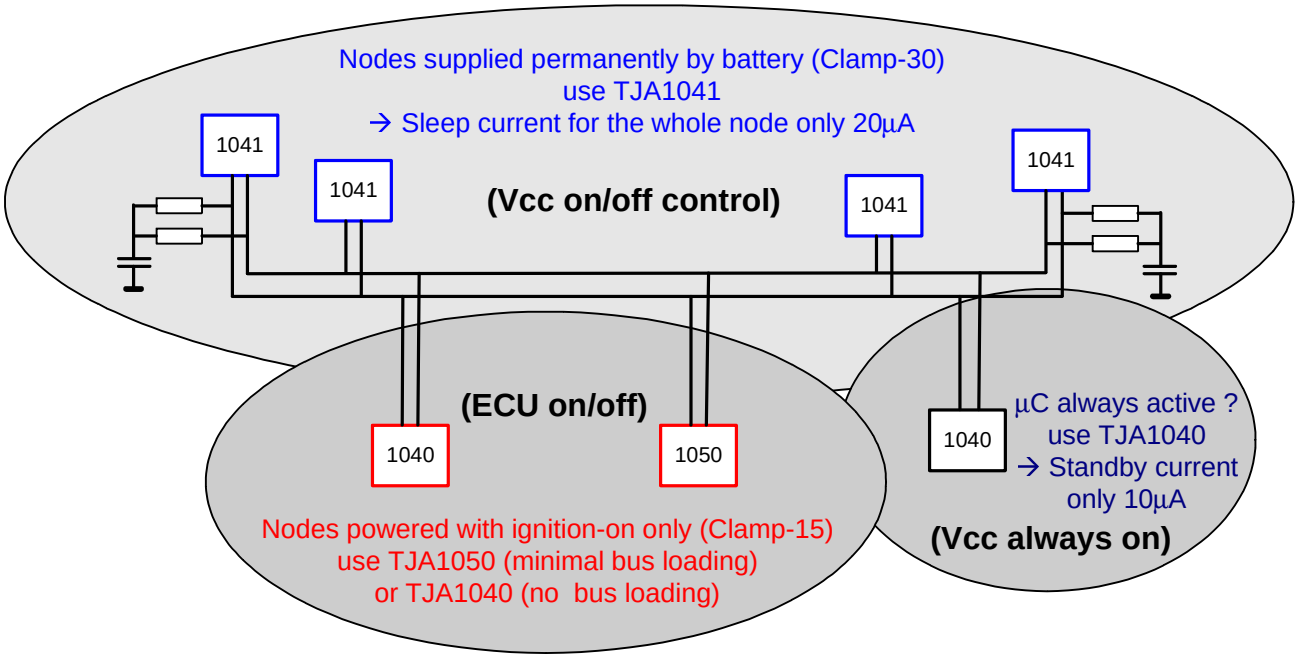


Figure 3-1: Target applications for the TJA1041 and TJA1040/1050

1. Applications, which have to be available all time, even when the car is parked and ignition-key is off, are permanently supplied from a permanent battery supply line, often called “Clamp-30”. However, those nodes need the possibility to reduce the current consumption for saving the battery. Here, the TJA1041 is the preferred transceiver as it allows to put the node in a Sleep Mode, which allows reducing the total current consumption of the node down to typ. 20µA, while keeping the capability to receive wakeup events from the bus and to restart the application. In these applications the TJA1041 takes control over the ECU internal power supply and wakeup requirements.
2. Applications, which do not need to be available with ignition-key off, are simply switched off and become totally un-powered during ignition-key off. They are supplied from a switched battery supply line, often called “Clamp-15”. This supply line is switched off with ignition-key off. Those nodes do not need enhanced low-power management. Depending on system requirements, e.g. partial communication of the still supplied nodes during “ignition key off”, these un-powered nodes need to behave passive towards the remaining bus. Here, the TJA1050 and the TJA1040 are the preferred

transceivers. While the TJA1050 allows still some minor reverse current from the bus, the TJA1040 provides a perfect floating behaviour at the bus terminals CANH and CANL when un-powered.

3. There are also applications, which need an always-active microcontroller. Those nodes are permanently supplied from the permanent battery supply line “Clamp-30” and therefore they need also the possibility for current consumption reduction but without disabling a local voltage supply. Here, the TJA1040 is the preferred transceiver. In order to save current, the microcontroller can put the TJA1040 into Standby Mode reducing the Vcc supply current to a minimum. The still supplied microcontroller might enter a power-down mode too or disable the voltage supply of the transceiver. In the latter case the microcontroller takes control over the ECU internal power supply and wakeup requirements.

4. NEW FEATURES

Today modern bus implementations call increasingly for low system power consumption, high system reliability, excellent EMC (Electromagnetic Compatibility) and flexible interfacing. The new features of the TJA1041, shown in Figure 4-1, reflect this increasing demand on bus transceiver.

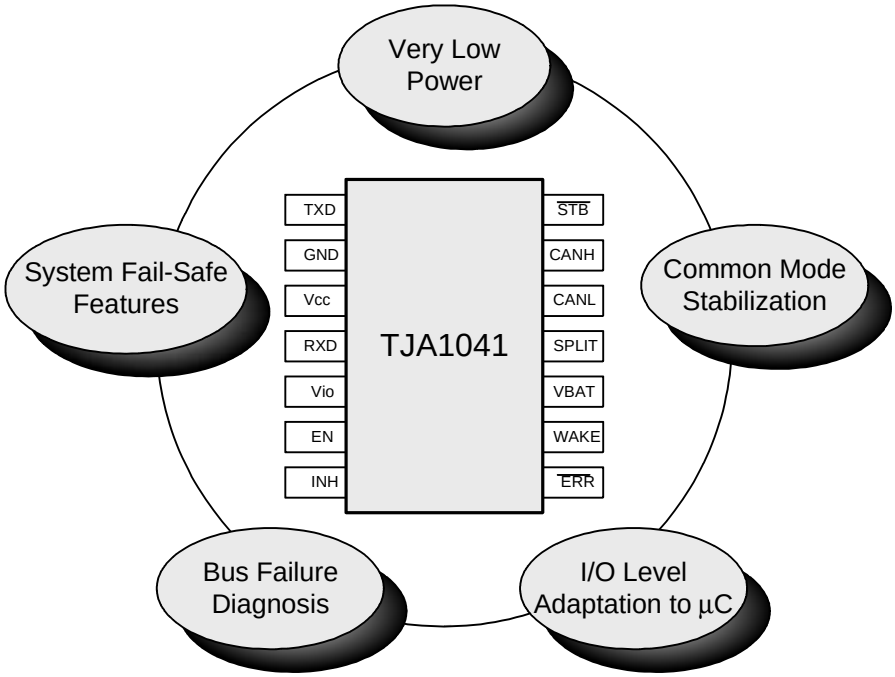
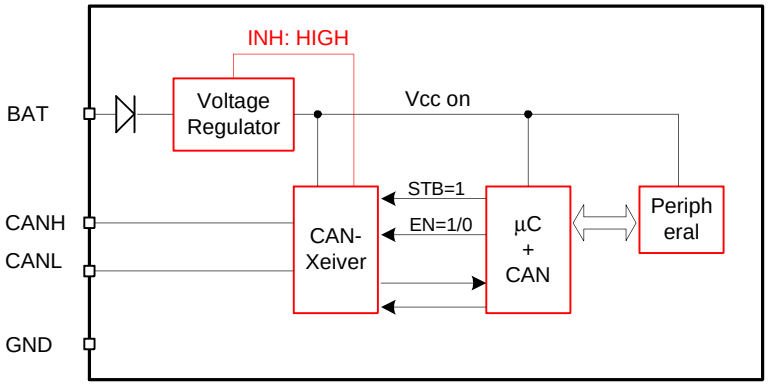


Figure 4-1: The new features of the TJA1041

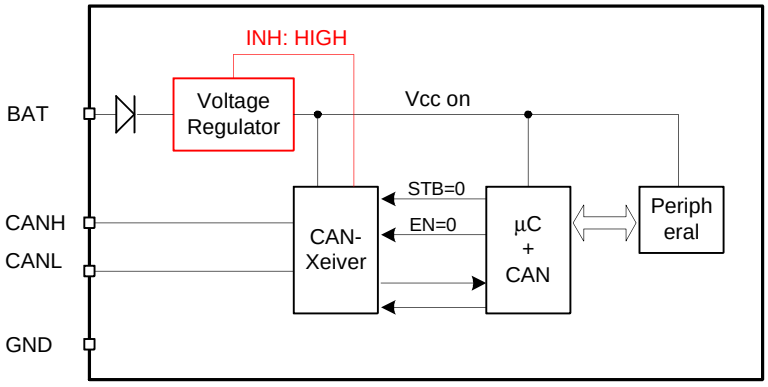
4.1 Low Power Management

Modern in-vehicle networking architectures require the availability of the CAN high-speed bus even when ignition key is off. As more and more nodes are introduced and thus need to be supplied by the battery in this case, the quiescent ECU current consumption has to be as low as possible. Otherwise the battery would be discharged within a short time while the car is parked. The low power management of the TJA1041 allows reducing the quiescent current consumption of a complete node to about typ. 20µA. This current consumption is low enough to allow permanent battery supply of the transceiver and thus keeping wakeup capability via the bus available. This way the system is able to react on local events as well as on CAN messages, resulting in wakeup of the complete bus system.

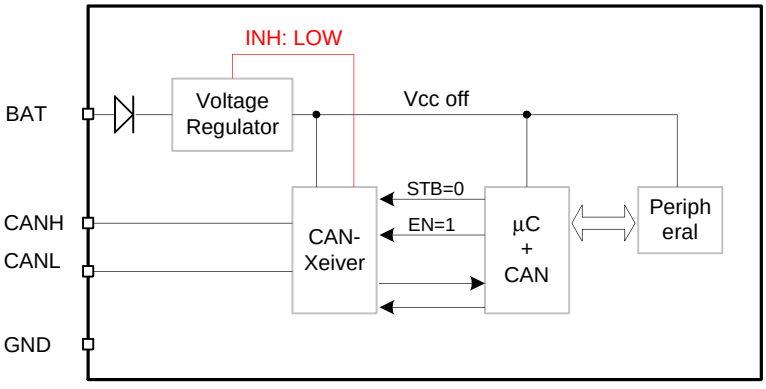
The operating modes of the TJA1041 (Normal, Pwon/Listen-Only, Standby, Sleep) establish a low power management with three different levels as sketched in Figure 4-2 and Table 4-1. In level 0 the ECU components (voltage regulator, microcontroller, transceiver, peripherals) are active and powered (indicated with red boxes in Figure 4-2). The TJA1041 is either in Normal or Pwon/Listen-Only Mode. The transceiver and the host microcontroller are powered by the active Vcc supply.



A) TRX in Normal/Pwon-Listen-Only Mode (Low-power level 0)
uC and peripheral are powered by Vcc and active



B) TRX in Standby Mode (Low-power level 1)
uC and peripheral are powered by Vcc, but may be in power-down mode



C) TRX in Sleep Mode (Low-power level 2)
uC and peripheral are typically un-powered

Figure 4-2: Low-power management of TJA1041

The next level of low power, level 1, is achieved with the TJA1041 operating in Standby Mode. The microcontroller, transceiver and peripherals are still powered by the active Vcc supply, but the functionality is often reduced to a minimum in order to save current. In case of the TJA1041 the function is reduced to detection of wakeup events only. Transmit and receive function as provided in Normal Mode is not available. The host microcontroller is often put in a power-down condition in order to save additional current.

The low power level 2 is associated to the Sleep Mode of the TJA1041. In Sleep Mode the external voltage regulator(s), supplying the transceiver and host microcontroller, is (are) typically switched off via the INH output signal of the transceiver. Thus the Vcc supply for the transceiver and microcontroller is not available. While the host microcontroller and peripherals are completely un-powered, the TJA1041 keeps powered via the battery supply pin "V_{BAT}". This supply is needed to ensure wakeup capability either via the bus or via a local wakeup event. The low power level 2 guarantees the lowest current consumption of a node.

Low Power Level	Operating Mode	Vcc Supply	µC	Node Power Consumption
Level 0 (Bus active)	Normal, Pwon/Listen-Only	Active	Powered	Normal
Level 1	Standby	Active	Powered	Low
Level 2	Sleep	Off	Un-powered	Very low

Table 4-1: Characteristics of the different low power levels

4.2 Bus Failure Diagnosis

While physical bus failures normally lead to interruption of bus communication, there are certain bus failures that are tolerated within the physical layer of CAN High-Speed. Without the bus failure diagnosis feature of the TJA1041 the application microcontroller would not have a chance to become aware of these bus failures. Apart from increasing current consumption, those bus failures are responsible for poor EMC performance and thus have to be avoided. The TJA1041 is able to detect bus wire short circuits, including those described above. For bus failure signalling to the microcontroller the TJA1041 provides the Bus Failure flag.

4.3 System Fail-Safe Features

The motivation was to create a fail-safe system, which is able to detect and handle failure scenarios critical to the bus operation such that the remaining bus system will not be affected. There are several local failure scenarios like pin short circuits, which may result in a state in which the bus communication is heavily disturbed or even interrupted. With the TJA1041 the impact of those local failures remains confined to the corrupted node only, without degradation of bus communication between the other nodes. For local failure signalling to the microcontroller the TJA1041 provides the Local Failure flag.

4.4 Common Mode Stabilization

The high impedance characteristic of the bus during recessive state makes the bus vulnerable to the presence of even small leakage currents, which may occur in case of un-powered ECUs within the bus

system. As a result the common mode voltage can show a significant voltage drop from the nominal Vcc/2 value. The TJA1041 provides means for common mode stabilization by offering a voltage source of nominal Vcc/2 at the pin "Split". Without that feature leakage currents would result in significant drop of the common mode voltage during recessive state. Upon subsequent transmitting of the first dominant bit of a CAN-message (Start-of-Frame Bit) the common mode voltage would restore to its nominal value, leading to a large common mode step and thus increasing emission. In fact the common mode stabilization of the TJA1041 significantly improves the EMC performance even if there are un-powered ECUs on the bus.

4.5 I/O Level Adaptation to Host Controller Supply Voltage

As the TJA1041 supports the physical layer of the ISO11898 standard, it needs a +5V supply voltage as reference voltage. On the other hand, modern microcontroller ICs often require supply voltages lower than 5V, mostly +3.3V and less.

The TJA1041 provides a continuous threshold level adaptation for the interface pins to the microcontroller down to a microcontroller supply voltage of 2.8V [1]. For this purpose the host controller supply voltage is connected to the transceiver pin "V_{IO}" to provide the reference voltage for the input/output interface. It defines the ratiometric digital input threshold for TXD, EN and $\overline{\text{STB}}$ and the HIGH-level output voltage for RXD and $\overline{\text{ERR}}$. Due to this function the transceiver can be interfaced to any microcontroller with a typical supply voltage between 2.8V and 5V.

5. OPERATING MODES

The TJA1041 provides five different operating modes, which are controlled by the input pins "$\overline{STB}$" and "EN". The reference state diagram for the operating modes can be found in the data sheet [1]. In case of an undervoltage condition on the pin Vcc or V_{IO} , the transceiver is forced into Sleep Mode, thus overruling the current mode selection at the pins "$\overline{STB}$" and "EN". In case of an undervoltage condition on the pin “VBAT” the transceiver is forced into Standby Mode.

Depending on the operating mode the transceiver shows different behaviour for the receiver and bus driver as well as on output pins like "$\overline{ERR}$" and "RXD". Table 5-1 summarizes the characteristics in each operating mode.

5.1 Normal Mode

For CAN communication the Normal Mode is chosen. The digital bit stream input at TxD is transferred into corresponding analog bus signals. Simultaneously, the transceiver monitors the bus, converting the analog bus signals into the corresponding digital bit stream output at RxD. The external voltage regulator is active, the bus lines are biased to Vcc/2 and the transmitter is enabled. The Normal Mode is entered setting $\overline{STB}$=1 and EN=1.

5.2 Pwon/Listen-Only Mode

The Pwon/Listen-Only Mode has in general two different functions. First, as the name suggests, it realizes a Listen-Only behaviour. The node is only allowed to receive messages from the bus but not to transmit onto the bus. The digital bit stream from the CAN-controller at TxD is simply ignored. In this way a node can be prevented from influencing the bus.

Second, the Pwon/Listen-Only Mode provides the Local Failure flag and PWON flag at the pin "$\overline{ERR}$", which can be read by the microcontroller. For flag signalling at the pin "$\overline{ERR}$" refer to chapter 7. The Pwon/Listen-Only Mode is entered setting $\overline{STB}$=1 and EN=0.

5.3 Standby Mode

The Standby Mode is used to achieve the low power level 1. The power consumption of the TJA1041 is significantly reduced compared to Normal or Pwon/Listen-Only Mode. In Standby Mode the TJA1041 is not capable of transmitting and receiving regular CAN messages. However, the TJA1041 monitors the bus for CAN messages. Whenever a dominant phase of longer than t_{BUS} [1] is detected on the bus, indicating bus traffic, the internal Wakeup flag is set. The TJA1041 can also receive a local wakeup via the pin "WAKE". Upon detection of a remote or local wakeup the internal Wakeup flag is set. In Standby Mode this flag is output at the pins "$\overline{ERR}$" and "RXD". To reduce the current consumption as far as possible the bus is terminated to GND rather than biased to Vcc/2 as in Normal or Pwon/Listen-Only Mode. The Standby Mode is selected with $\overline{STB}$=0 and EN=0.

5.4 Sleep Mode

The Sleep Mode is used to achieve the low power level 2. While the transceiver current consumption is the same as in Standby Mode, it allows further reduction of the system current consumption by switching off the external voltage regulator (Vcc supply) for the transceiver, host microcontroller etc.

The only way to put the TJA1041 into Sleep Mode is using the Goto Sleep Command Mode ($\overline{STB}$=0, EN=1). If it is selected for longer than the "minimum hold time of go-to-sleep command" $t_{h(min)}$ [1], the transceiver is automatically forced into Sleep Mode switching the pin "INH" to floating.

The only difference between the Sleep and the Standby Mode concerns the pin "INH". It provides a battery related open drain output to control one or more external voltage regulators. In Sleep Mode the pin "INH" is set floating compared to a "HIGH" signal (V_{BAT}-based) in all other modes (also Standby Mode), thus typically disabling the voltage regulator(s) for the transceiver and microcontroller. While the microcontroller is completely un-powered (no Vcc supply), the TJA1041 keeps partly alive via the battery supply. It allows the transceiver to monitor the bus for CAN messages. In fact, the transceiver is the device controlling autonomously the Vcc supply for the ECU.

Wakeup from Sleep Mode is generally possible via two channels:

- Wakeup via a dominant bus state
- Local wakeup via an edge at pin “WAKE”

Upon wakeup, the pin "INH" goes "HIGH" enabling the external voltage regulator(s) again. The wakeup flag is set in case of a local or remote wakeup. It is reflected at the pins "$\overline{\text{ERR}}$" and "RXD". As in Standby Mode, the bus lines CANH and CANL are terminated to GND. Table 5-1 summarizes the characteristics of the TJA1041 in the different operating modes.

A continuous bus condition, where one part of the nodes is in Normal or Pwon/Listen-Only Mode while the other part is in Standby or Sleep Mode, should be avoided due to the different bus biasing in these modes. Otherwise a continuous DC common mode current would flow from one part to the other.

A mode transition from Sleep mode to any other mode via $\overline{\text{STB}}$ and EN is possible only if the supply voltage Vcc and V_{IO} were present all time during Sleep mode. Once a Vcc or V_{IO} under-voltage was detected, any mode control via $\overline{\text{STB}}$ and EN is disabled for fail-safe reasons. This feature helps to prevent the microcontroller from continuously waking up the transceiver via $\overline{\text{STB}}$ and EN in case a Vcc or Vio under-voltage has been detected by the transceiver.

5.5 Go-to Sleep Command Mode

The Go-to-Sleep Command Mode has the meaning of a command rather than the meaning of a typical operating mode. It is used to put the TJA1041 into Sleep Mode. Due to the spread of the "minimum hold time of go-to-sleep command" $t_{h(min)}$ [1] the Go-to Sleep Command Mode must be actually selected for longer than the maximum value in order to make sure the Sleep Mode will be entered reliably. Immediately after selecting the Go-to Sleep Command Mode the transmitter is disabled, the bus lines are terminated to GND and the Wakeup flag information is signalled at the pins "$\overline{\text{ERR}}$" and "RXD". The Go-to Sleep Command Mode is selected with $\overline{\text{STB}}$=0 and EN=1.

Note, that the Go-to Sleep Command might become overruled by a wake-up event, if this wake-up event occurs simultaneously with the Go-to Sleep Command. In this case, the wake-up will be signalled on RXD and $\overline{\text{ERR}}$ as desired, while INH stays active HIGH.

Operating Mode	$\overline{STB}$	EN	$\overline{ERR}$-Pin		RXD-Pin		Bus Bias	INH-Pin
			LOW	HIGH	LOW	HIGH		
Normal	1	1	Bus Failure flag set (note 1)	Bus Failure flag reset (note 1)	Bus dominant	Bus recessive	Vcc/2	V_{BAT}
			Wakeup Source flag; local wakeup detected (note 2)	Wakeup Source flag; remote wakeup detected (note 2)				
Pwon/ Listen-only	1	0	PWON flag set; (note 3)	PWON flag reset; (note 3)	Bus dominant	Bus recessive	Vcc/2	V_{BAT}
			Local Failure flag set (note 4)	Local Failure flag reset (note 4)				
Go-to Sleep Command	0	1	Wakeup flag set (note 5)	Wakeup flag reset (note 5)	Wakeup flag set (note 5)	Wakeup flag reset	Ground	V_{BAT}
Standby	0	0						V_{BAT}
Sleep; note 6	0	X						float

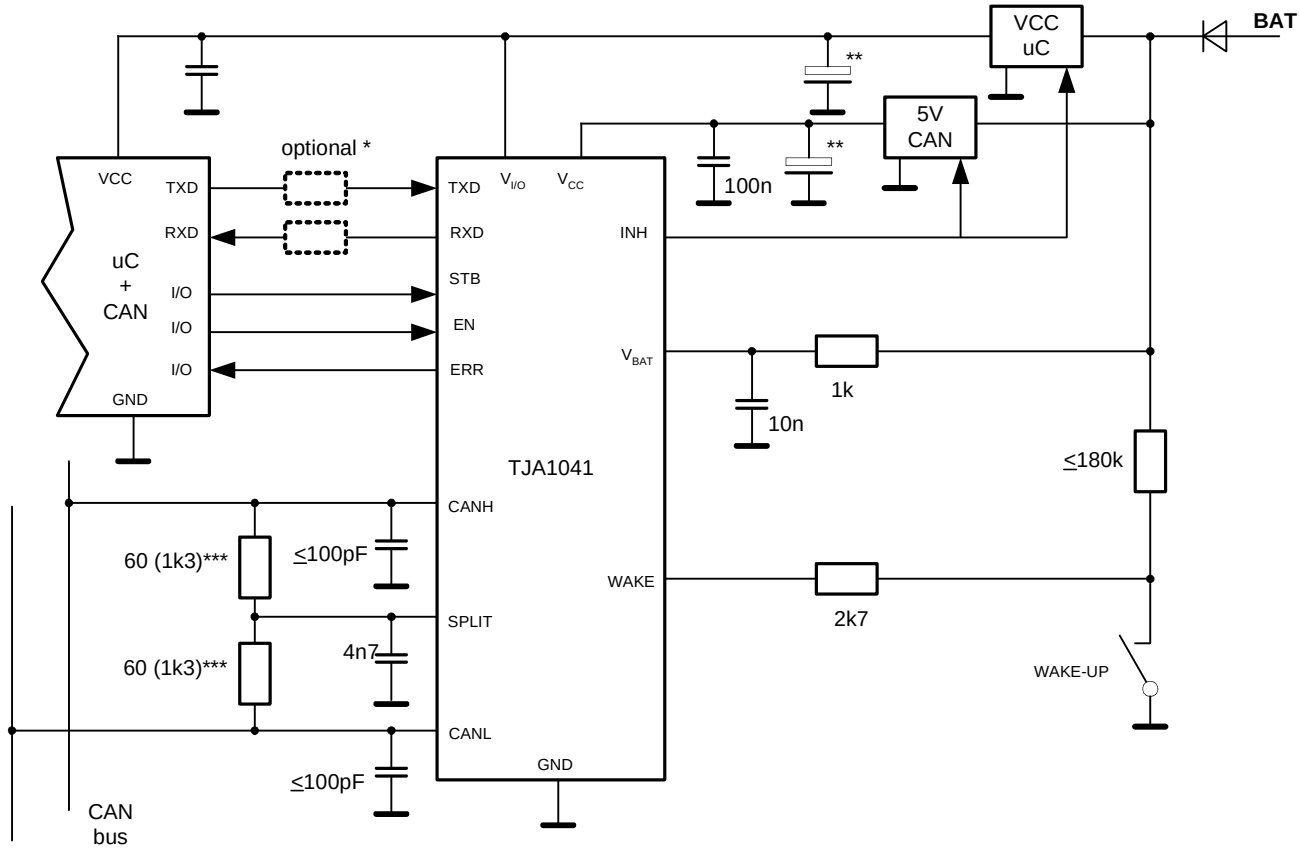
Note

1. Valid after the 4th dominant to recessive edge at TXD after entering the Normal Mode (each dominant period should be at least 4µs)
2. Valid before the 4th dominant to recessive edges at TXD after entering the Normal Mode
3. Valid if $V_{I/O}$ are present and coming from Sleep, Standby or Go-to Sleep Command Mode
4. Valid if $V_{I/O}$ are present and coming from Normal Mode
5. Valid if $V_{I/O}$ is present
6. Transceiver will enter the Sleep Mode only if the Go-to Sleep Command Mode was selected longer than the hold time of go-to-sleep command ($t_{h(min)}$) or by an under-voltage detection on Vcc or $V_{I/O}$.

Table 5-1: Characteristics of the different operating modes

6. HARDWARE APPLICATION OF THE TJA1041

Figure 6-1 shows how to integrate the TJA1041 within a typical application. The application example assumes a 3.3V supplied host microcontroller. There is a dedicated 5V regulator supplying the TJA1041 transceiver and a dedicated 3.3V regulator supplying the microcontroller. Both voltage regulators are controlled via the INH output of the transceiver, so that in Sleep Mode both voltage regulators are switched off. Furthermore, the application example makes use of the pin "WAKE" for local wakeup possibility, connecting it to a low-side switch. This example illustrates a typical application of the TJA1041.



* For further EMC optimization a series resistor could be applied in case the bus timing parameters allow this additional delay caused by the additional R/C time constant.
** Size of capacitor depends on regulator.
*** For stub nodes a "weak" termination improves the EMC behaviour of the system in terms of emission.

Figure 6-1: Typical application for 3.3V microcontroller

6.1 Pin V_{BAT}

The battery supply ensures the local and remote wakeup capability of the TJA1041 when the Vcc supply is switched off during Sleep Mode. Nevertheless the current consumption I_{BAT} via this pin is very low [1]. It is recommended to place a series resistor of 1kΩ into the battery supply line of the transceiver for enhanced protection against automotive transients. Given the max. supply current I_{BAT} of 40µA at V_{BAT}, a voltage drop of 40mV must be taken into account when determining the minimum battery operating voltage. In

addition, a capacitor of about 10nF, closely connected to the V_{BAT} pin and forming a low-pass filter in conjunction with the series resistor, can be used for enhanced transient protection.

6.2 Pin Vcc

The Vcc supply via pin “Vcc” provides the current needed for the transmitter and receiver of the TJA1041. The Vcc supply must be able to deliver current of 68mA in average for the transceiver (see Appendix 13.2). Using a linear voltage regulator, it is recommended to stabilize the output voltage with a bypass capacitor of about 20µF (see Appendix 13.2). This type of capacitor should be connected at the output of the voltage regulator. In addition, a second capacitor should be connected as close as possible between pin “Vcc” and “GND” of the transceiver. Its function is to buffer the Vcc supply voltage, especially during fast load changes at a transition from recessive to dominant. Recommended value is 47-100nF. For reliability reasons it might be useful to apply two capacitors in series connection between Vcc and GND. Thus, a single shorted capacitor (e.g. damaged device) cannot short-circuit the Vcc supply.

6.3 Pin Vio

The pin "Vio" is connected to the µC supply voltage to provide the proper voltage reference for the input threshold of digital input pins and for the "HIGH" voltage of digital outputs. Unlike other products on the market, the TJA1041 provides a continuous level adaptation from as low as 2.8V to 5V. The level adaptation applies to all interface pins between the microcontroller and the transceiver, i.e. TxD, EN, $\overline{STB}$ (input pins) and RxD, $\overline{ERR}$ (output pins). In Normal Mode only a negligible small current $I_{I/O}$ [1] is drawn out of the battery supply. In Sleep Mode no current will be drawn via this pin. If the pin "Vio" is disconnected, an under-voltage condition on "Vio" will be detected and the transceiver is forced into Sleep Mode in order to provide defined fail-safe low-power system behaviour.

6.4 Pin TXD

The transceiver receives the digital bit stream to be transmitted onto the bus via the pin “TXD”. Sometimes signals at TXD show steep edges at bit transitions, likely to degrade the EMC performance. In this case, it is recommended to place a series resistor of about 1kΩ into the TXD line between transceiver and microcontroller. Along with pin capacitance this would help to smooth the edges to some degree. For high bus speeds (close to 1Mbit/s) the additional delay within TXD has to be taken into account.

6.5 Pin RXD

The analog bit stream received from the bus is output at pin “RXD” for further processing within the CAN-controller. As with pin “TXD” a series resistor of about 1kΩ can be used to smooth the edges at bit transitions. Again the additional delay within RXD has to be taken into account, if high bus speeds close to 1Mbit/s are used.

6.6 Pin $\overline{STB}$

The pin “$\overline{STB}$”, used for mode control along with pin “EN”, is typically connected to an output port pin of the microcontroller.

6.7 Pin EN

The pin “EN”, used for mode control along with pin “$\overline{STB}$”, is typically connected to an output port pin of the microcontroller.

6.8 Pin $\overline{\text{ERR}}$

The pin "$\overline{\text{ERR}}$" is a push-pull output stage for signalling failure conditions to the microcontroller. It is typically connected to an input port pin of the microcontroller. (see [1] for drive capability)

6.9 Pin CANH/L

The transceiver is connected to the bus via pin CANH/L. Nodes connected to the bus end must show a differential termination, which is approximately equal to the characteristic impedance of the bus line in order to suppress signal reflection. Instead of a one-resistor termination it is highly recommended using the so-called Split Termination, illustrated in Figure 6-1. EMC measurements have shown that the Split Termination is able to improve significantly the signal symmetry between CANH and CANL, thus reducing emission. Basically each of the two termination resistors is split into two resistors of equal value, i.e. two resistors of 60Ω instead of one resistor of 120Ω. The special characteristic of this approach is that the common mode signal, available at the centre tap of the termination, is terminated to ground via a capacitor. Recommended value for this capacitor is 4,7nF. Nodes connected to the bus via stubs do not need to have an extra differential termination. However, for stub nodes a "weak" termination (2x1k3) improves the EMC behaviour of the system in terms of emission.

As the symmetry of the two signal lines is crucial for the emission performance of the system, the matching tolerance of the two termination resistors should be as low as possible (desired: <1%).

Also depicted in Figure 6-1, it is recommended to load the CANH and CANL pin each with a capacitor of about 100pF close to the connector of the ECU. The main reason is to increase the robustness to automotive transients and ESD. The matching tolerance of the two capacitors should be as low as possible.

6.10 Pin SPLIT

In Normal and Pwon/Listen-Only Mode the pin "SPLIT" provides an output voltage of Vcc/2. In all other modes the pin is in high-ohmic state. By simply connecting the pin "SPLIT" to the center tap of the Split Termination as shown in Figure 6-1, DC stabilization of the common mode voltage is achieved.

Especially in case of un-powered nodes leakage currents from the bus into the transceiver may force the common mode voltage to drop below Vcc/2 during recessive state. The DC stabilization aims to oppose this effect of degradation and thus helps improving the emission performance. In case of no significant leakage currents from the bus, the pin "SPLIT" can be simply left open.

According to the data sheet [1] the min. impedance of the voltage source can be calculated to 2000Ω.

6.11 Pin WAKE

The pin "WAKE" can be used to signal a local wakeup event to the transceiver. Like for the Fault-tolerant CAN Transceiver TJA1054 [5] a signal change of sufficient length at the pin "WAKE" generates a local wakeup. While the TJA1054 features an internal pull-up to battery voltage to allow the use of a low-side switch, the pin "WAKE" of the TJA1041 features a variable biasing. Depending on the external biasing the internal one switches from GND to battery level or vice versa. Figure 6-2 illustrates the biasing concept of the TJA1041 along with different external switching circuits.

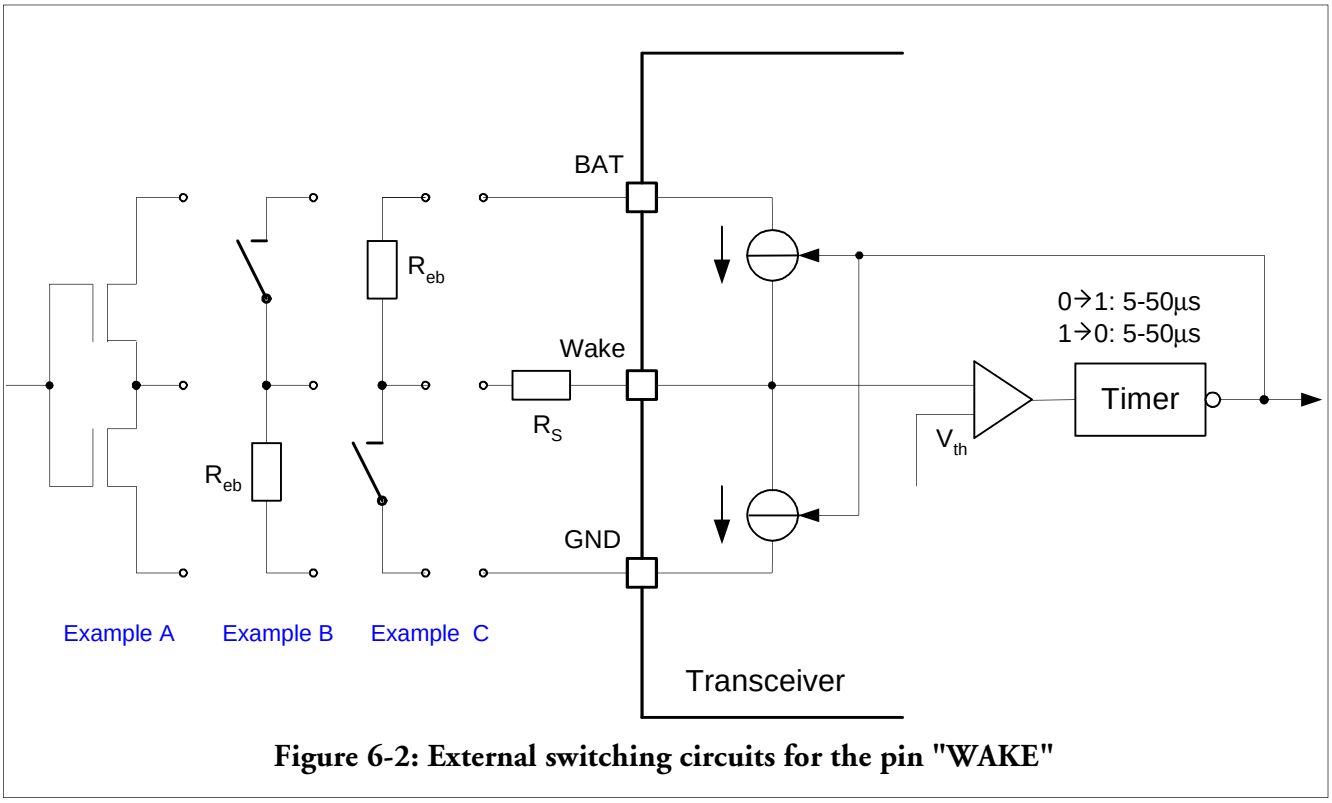


Figure 6-2: External switching circuits for the pin "WAKE"

If a voltage higher than the "Wakeup Threshold Voltage" $V_{th(WAKE)}$ [1] is held at the pin "WAKE" for longer than the maximum time t_{WAKE} [1], the internal biasing (current source) will switch reliably to battery level if the pin was at "LOW" level before. Similarly, if a voltage lower than this value is held for longer than the max. t_{WAKE} time, the internal biasing (current source) will switch reliably to GND if the pin was at "HIGH" level before. In fact the internal biasing is adapted automatically to the external biasing conditions. This concept allows using a low-side switch as well as a high-side switch or a V_{BAT} based push-pull stage without forcing undesired bias currents while there is no wakeup event.

In case of a low-side switch the resistor R_{eb} and the internal current source both provide a pull-up to Vbat. In order to launch a local wakeup the external switch has to be closed producing a negative pulse at the pin "WAKE". The negative pulse will pass the internal timer and release a wakeup reliably if the pulse is longer than the maximum value of t_{WAKE} [1]. Along with passing the timer the bias switches to GND. After releasing the low-side switch the external pull-up resistor switches the internal bias back to V_{BAT}. The resistor R_{eb} determines the current through the external switch when it is closed and is needed to guarantee a proper switch contact.

In case the pin “WAKE” is not used, it is recommended to connect the pin directly to ground level.

6.11.1 Dimensioning of R_S and R_{eb}

The purpose of the series resistor R_S is to protect the transceiver in case the ECU has a loss of ground situation while the wakeup switch still is connected to a proper GND. The minimum required series resistor is determined by the expected maximum battery supply voltage $V_{BAT,max}$ and the maximum allowed

current at pin “WAKE” of 15mA. The resistor should make sure that the current does never exceed this level. The minimum required series resistor R_S can be calculated by

$$R_{S,\min} = \frac{V_{BAT,\max}}{I_{Wake,\max}}$$

Assuming that V_{BAT} will not exceed 40V DC the series resistor should have a value of 2,7kΩ.

The resistor R_{eb} is needed to bring the bias back to its default state after the external switch has been applied. That defines an upper limit for the resistor value. For example, in case of a low-side switch the resistor R_{eb} together with the series resistor R_S must pull the pin "WAKE" above the switching threshold of the pin "WAKE". The equation for determining the upper limit for R_{eb} is

$$(R_{eb} + R_S) \cdot I_{Pull,\max} < V_{BAT} - V_{th(Wake),\max}$$

With the maximum pull-down (pull-up) current of 10μA and the maximum threshold of $V_{th(WAKE)}$, the upper limit for R_{eb} calculates to about 180kΩ.

6.12 Pin INH

The intention of the pin "INH" is to control one or more voltage regulators within the ECU. In Figure 6-1 two voltage regulators, one 5V regulator for the transceiver and one 3.3V regulator for the microcontroller, are controlled via the INH output of the transceiver as an example.

The pin "INH" provides a battery related open drain output. During Sleep Mode it is floating. Due to the typical pull-down behaviour of the Inhibit input pin of common voltage regulators, this results in a "LOW" signal on the Inhibit input, typically disabling the voltage regulator(s). In all other operation modes the transceiver pin "INH" is actively pulled to battery voltage, thus enabling the external voltage regulator(s).

In case the pin “INH” is not used for voltage regulator switching, it can be simply left open.

7. FLAG SIGNALING

The TJA1041 provides five different flags to be signalled to the microcontroller. The status of the flags can be read by the microcontroller via the pin "$\overline{ERR}$". Which flag is actually signalled on the pin "$\overline{ERR}$" depends on the current operating mode and on the history. Figure 7-1 shows the flag signalling of the pin "$\overline{ERR}$".

Notice that when switching from one mode to another, it will take some time until the “new” flag will be signaled at pin “$\overline{ERR}$”. Therefore, for reading the pin “$\overline{ERR}$” by the application software, after a mode transition has been performed, it is recommended to introduce a wait time in the software of at least 10µs before reading the pin “$\overline{ERR}$”.

7.1 Wakeup flag

A wakeup event from the bus or the pin “WAKE” will set the Wakeup flag only if the wakeup event is received while the TJA1041 is in Sleep, Standby or Go-to Sleep Command Mode. In Normal or Pwon/Listen-Only Mode any wakeup event is ignored. The Wakeup flag is signalled at the pin "$\overline{ERR}$" during Sleep, Standby and Go-to Sleep Command Mode provided that Vcc and V_{IO} are present. A "LOW" level signals a wakeup request for the microcontroller, received either via the bus or via the pin “WAKE”. It is reset either when the Normal Mode is entered or when there was a BAT-Under-voltage condition detected. As long as the Wakeup flag is set, a Go-to Sleep Command is simply ignored and thus a transition into Sleep Mode is not possible. The Wakeup flag is also signalled at the pin "RXD" with the same polarity as described for the pin “$\overline{ERR}$”.

7.2 PWON flag

The PWON flag is signalled at the pin “$\overline{ERR}$” during Pwon/Listen-Only Mode when coming from Standby, Sleep or Go-to Sleep Command Mode. It is set to "LOW" level if there was a battery under-voltage condition. Thus, if the battery has been connected the first time to the pin "V_{BAT}" or if there was a temporarily battery under-voltage condition, this flag is set. The PWON flag is reset once the Normal Mode is entered. As long as the PWON flag is set, it is not possible to enter the Sleep Mode. After first battery supply the PWON flag is initialized to “set”, indicated by a “LOW” level at pin “$\overline{ERR}$”.

7.3 Wakeup-Source flag

Entering the Normal Mode the pin "$\overline{ERR}$" first reflects the Wakeup Source flag. A "LOW" level signals a local wakeup via the pin "WAKE", whereas a "HIGH" level indicates a wakeup via the bus. The Wakeup Source flag will be overwritten by the Bus Failure flag after the node has transmitted four recessive-to-dominant bit transitions in Normal Mode. Since the application is controlling its own transmission behaviour, the application has any time needed to read this Wakeup Source flag. The Wakeup Source flag is cleared and set to the default state "HIGH" whenever the Normal Mode is left. After first battery supply the Wakeup-Source flag is initialized to “wakeup via bus”, indicated by a “HIGH” level at pin “$\overline{ERR}$”.

7.4 Bus Failure flag

After the transceiver has transmitted four recessive-to-dominant bit transitions with a dominant bit length of at least 4µs , the Bus Failure flag will overwrite the Wakeup Source flag. A "LOW" level indicates a short circuit condition on the bus. The Bus Failure flag is reset to default "HIGH" whenever the Normal Mode is left. Thus, leaving the Normal Mode and re-entering the Normal Mode forces the pin "$\overline{ERR}$" to default state "HIGH", if there was no local wakeup meantime. Signalling the Bus Failure flag requires

again transmission of at least four recessive-to-dominant bit transitions. Detection of bus failures does not lead to a change of the transceiver operation. Active fault tolerance as known from the CAN Low-Speed Transceiver TJA1054 is not supported.

7.5 Local Failure flag

Entering the Pwon/Listen-Only Mode from the Normal Mode, the pin "$\overline{\text{ERR}}$" signals the Local Failure flag. A "LOW" level indicates those failures, which are associated with the local node only like

- TxD Dominant Clamping
- TxD/RxD Short Circuit
- RxD Recessive Clamping
- Bus Dominant Clamping
- Over-temperature Condition.

For a detailed description of the detected local failures refer to section 9. If any of these local failures is present, this will be indicated to the application by an active "LOW" signal. A more differentiated diagnosis is not supported. Along with setting the Local Failure flag the transmitter will be disabled due to fail-safe reasons, except for RxD Dominant Clamping detection. The Local Failure flag is reset and thus the transmitter enabled again either by forcing a transition into Normal Mode or by receiving a dominant bit from the bus while TxD is recessive.

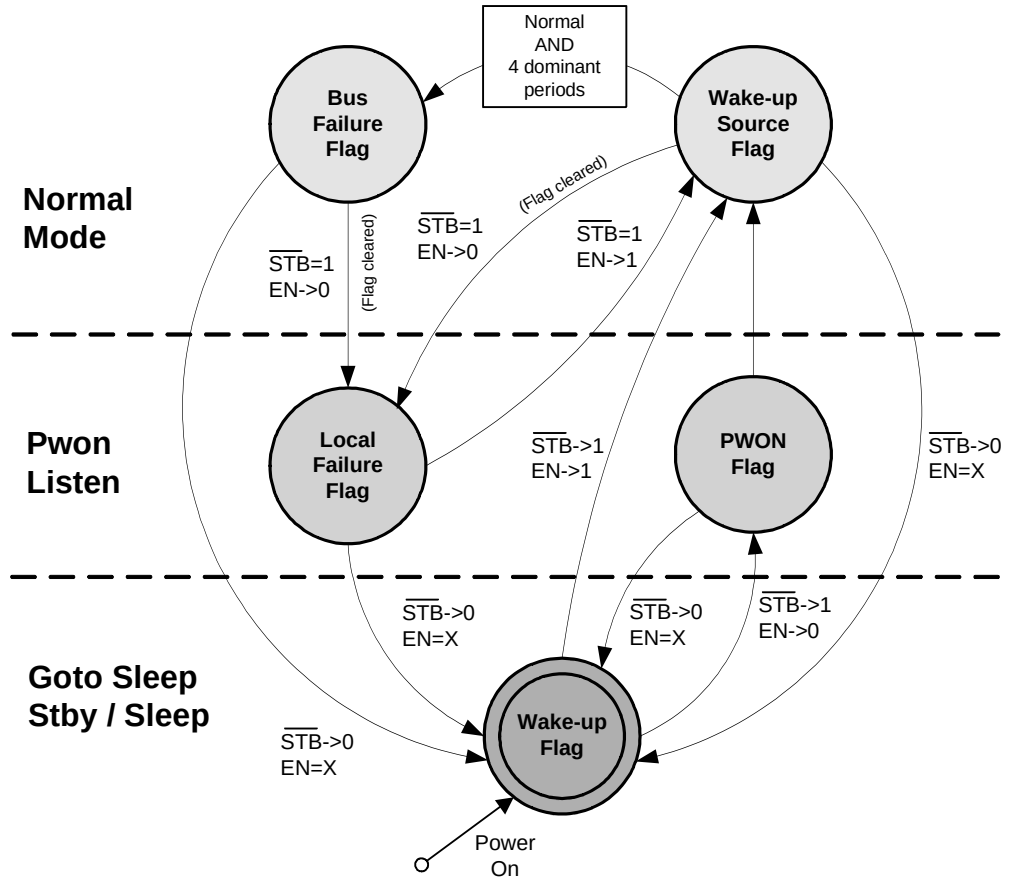


Figure 7-1: Flag signalling of the pin "$\overline{\text{ERR}}$"

8. BUS FAILURE DIAGNOSIS

8.1 List of signalled bus failures

Assuming a bus load of nominal 60Ω the following bus failure conditions are detectable by the TJA1041:

- CANH x BAT (communication still possible, “hidden” bus failure)
- CANH x Vcc (communication still possible, “hidden” bus failure)
- CANH x GND (communication not possible)
- CANL x BAT (communication not possible)
- CANL x Vcc (communication not possible)
- CANL x GND (communication still possible, “hidden” bus failure)

The listed short-circuits will be reliably detected in a range from 0 to 50Ω. A short-circuit between CANH and CANL or line interruption failures are not detected. For analyzing the bus the node needs to actively transmit onto the bus. Before the Bus Failure flag becomes valid, the node must have transmitted at least four dominant sequences onto the bus each of at least 4μs length.

As already mentioned in section 4.2, the bus system performance suffers from "hidden" bus failure conditions in terms of EMC. The "hidden" bus failures are a short-circuit CANHxBAT, CANHxVcc and CANLxGND. They will be normally tolerated by the CAN High-Speed Physical Layer as long as the capacitive load on the bus is not too large, otherwise dominant periods on the bus would lengthen at the expense of recessive periods, likely causing bit timing violations. Communication between nodes is still possible. Without additional diagnosis on physical layer level the microcontroller has no chance to get to know from those bus failures. The bus failure diagnosis aims to detect such failure conditions and to signal them to the application microcontroller.

8.2 How to read the Bus Failure Flag

The Bus Failure flag is actually signalled at the pin "$\overline{\text{ERR}}$". When entering the Normal Mode the pin "$\overline{\text{ERR}}$" first reflects the Wakeup-source flag. After four dominant periods of sufficient length have been transmitted, the Bus Failure flag gets active at the pin "$\overline{\text{ERR}}$".

During arbitration, when more than one node may transmit simultaneously the bus failure measurement process may be distorted, resulting in unstable bus failure information. Therefore, it is recommended that reading the Bus Failure flag from the microcontroller should take place at the end of the CAN frame only, e.g. within the transmit interrupt service routine. The read process should be completed before the transceiver is sending the next CAN message. In order to be able to guarantee the four needed dominant periods each of more than 4μs length, a dedicated diagnosis message with appropriate payload may be helpful, especially for high bit rates.

A possible flow diagram for the Transmit Interrupt Service Routine is shown in Figure 8-1. If reading of the pin "$\overline{\text{ERR}}$" indicates a "LOW" signal, a "hidden" bus failure must be present, because in case of bus failures, leading to complete corruption of communication, the Transmit Interrupt Service routine would never be reached.

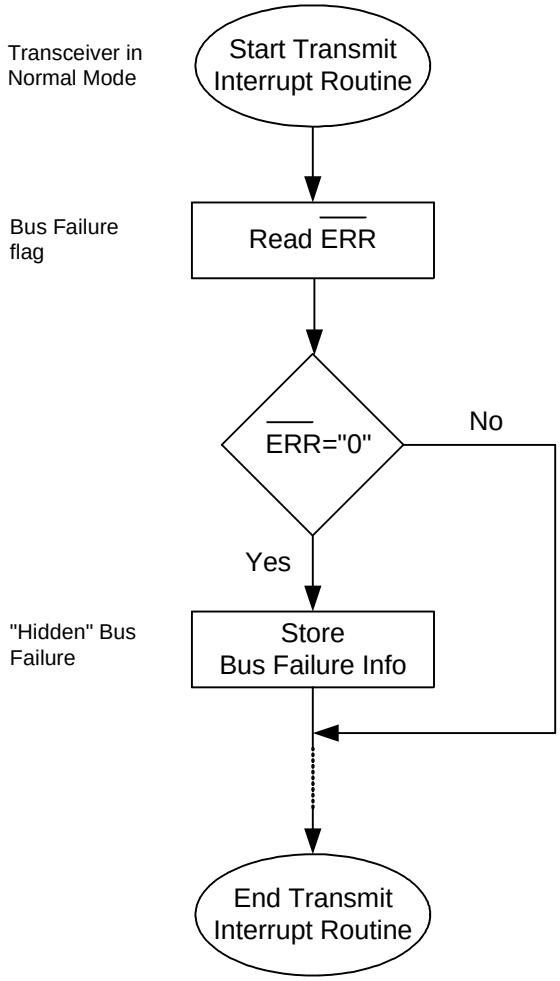


Figure 8-1: Flow diagram for the Transmit Interrupt Service Routine

9. LOCAL FAILURE DIAGNOSIS

Local failures detected and signalled at the pin "$\overline{\text{ERR}}$" in Pwon/Listen-Only Mode (when coming from Normal Mode) include:

- TxD Dominant Clamping
- TxD/RxD Short Circuit
- RXD Recessive Clamping
- Over-temperature

Upon detection of one of these local failures the Local Failure flag will be set and the transmitter will be disabled. Beside of the mentioned failures above, information about Bus Dominant Clamping is not stored with the Local Failure flag. However, it is also indicated at the pin "$\overline{\text{ERR}}$" during Pwon/Listen-Only Mode. No other measure is taken in case of Bus Dominant Clamping.

9.1 Recovery from Local Failures

Whenever the pin "RXD" becomes dominant while TxD is recessive, the Local Failure flag will be reset along with enabling the transmitter again. This indicates that a local failure like TxD Dominant Clamping, TxD/RxD Short Circuit or RxD Recessive Clamping does not exist any more. In Pwon/Listen-Only Mode failure recovery is immediately reflected on the pin "$\overline{\text{ERR}}$" going "HIGH" again.

Another way to reset the Local Failure flag and to enable the transmitter is forcing a transition into Normal Mode from any other mode. This reset option is necessary when there is no bus traffic i.e. the pin "RXD" does not become dominant. In this case the application microcontroller can force a transition to Normal Mode after it has read the error status in Pwon/Listen-Only Mode. If the failure is still present, it is detected again, thus disabling the transmitter. If on the other hand the failure has gone, normal operation is resumed. A suggested flow diagram for handling communication failures is shown in Figure 11-1.

9.2 TXD Dominant Clamping

This fail-safe feature is already known from the TJA1050 and described in the Application Note AN00020 [10]. It prevents an erroneous CAN-controller from clamping the bus to dominant level by a continuously dominant TxD signal.

After a maximum allowable TxD dominant time t_{DOM}(TXD) [1] the transmitter is disabled. According to the CAN protocol [2] only a maximum of eleven successive dominant bits are allowed on TxD (worst case of five successive dominant bits followed immediately by an error frame). Along with the minimum allowable TxD dominant time, this will limit the minimum bit rate to 40kbit/s.

9.3 TXD/RXD Short Circuit

Without the protection feature of the TJA1041, a TxD/RxD short circuit would result in a dead-lock situation clamping the bus dominant. If for example the transceiver receives a dominant signal, RxD will output a dominant level. Due to the short circuit, TxD will then reflect a dominant signal too, thus keeping the dominant bus state. As a result TxD and hence the bus are clamped continuously dominant. The resulting effect is the same as for the continuously clamped dominant TxD signal. Thus the TxD dominant timeout will interrupt the dead-lock situation by disabling the transmitter. The bus and also TxD become recessive again. However, the failure scenario may still exist and with the next dominant

signal on the bus the described procedure will start again. Apparently, the TxD dominant timeout alone is not sufficient to protect the bus from a local TxD/RxD short circuit.

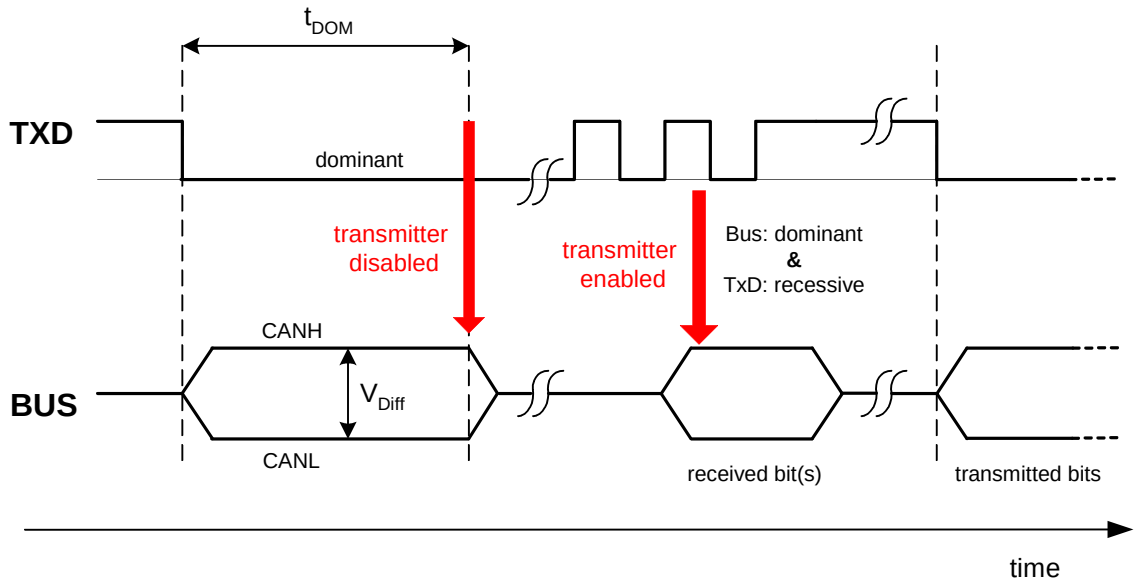


Figure 9-1: TXD Dominant Timeout and recovery mechanism

The TJA1041 keeps the transmitter off after detection of a TXD dominant clamping even if TxD gets released again. Failure recovery is performed first if the transceiver has detected a dominant bus signal while TxD is recessive. This is a clear indication that the TxD/RxD short circuit has gone. Figure 9-1 illustrates the disabling and enabling of the transmitter with respect to a TxD/RxD short circuit. In this way it is guaranteed that a local TxD/RxD short circuit will not disturb the communication of the remaining bus system.

9.4 RXD Recessive Clamping

If the pin "RXD" is shorted to Vcc or Vio, the pin "RXD" will be clamped to recessive signal. Using a conventional transceiver such a node assumes that the bus is permanently in Idle State. Therefore, it will launch a message transmission on the bus whenever it wants regardless of other bus traffic. As a result the bus traffic will be heavily disturbed.

The TJA1041 is able to detect a RXD Recessive Clamping situation whenever it receives a dominant bus signal. Upon detection the transmitter will be disabled immediately, so that the corrupted, not-synchronised node will be prevented from disturbing the remaining bus traffic. Of course, then the corrupted node is excluded from communication. It can neither transmit nor receive any message, whereas the remaining bus is unaffected.

9.5 Bus Dominant Clamping

In case of a short circuit from CANH to BAT/Vcc, the circuit for the Common Mode Stabilization may produce a differential voltage on the bus between CANH and CANL even if there is no dominant

transmitting node. This is illustrated in Figure 9-2. The differential voltage can be high enough to represent a dominant signal (V_{diff} > 0,9V). The result may be a permanently dominant clamped bus in case of a short circuit from CANH to BAT.

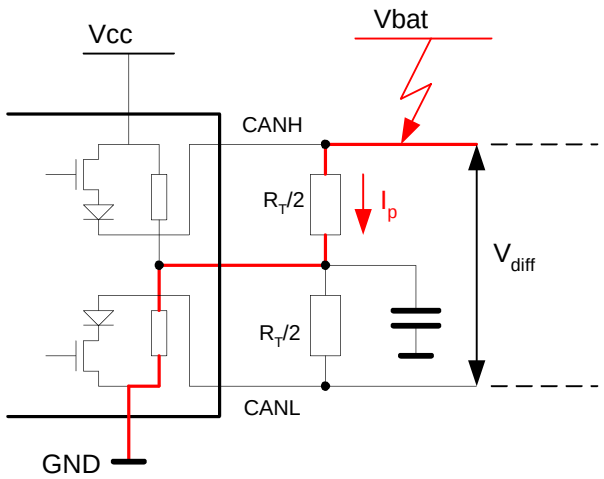


Figure 9-2: Bus Dominant Clamping in case of a short circuit from CANH to BAT

The TJA1041 is able to detect and report a Bus Dominant Clamping situation. If the receiver detects a bus dominant phase of longer than the "bus dominant time out" t_{DOM}(bus) [1] , this will be indicated at the pin "$\overline{ERR}$" in Pwon/Listen-Only Mode.

9.6 Over-Temperature Protection

An over-temperature condition may occur either if the transceiver is operated in an environment with high ambient temperature or if there is a short circuit condition on the bus. To protect the transceiver from self-destruction the transmitter will be disabled automatically whenever the junction temperature exceeds the allowed limit [1]. In addition the Local Failure flag will be set, which can be read at the pin "$\overline{ERR}$" in Pwon/Listen-Only Mode.

After an over-temperature condition the transmitter of the TJA1041 is released if the junction temperature is below the limit and if there is a transition into Normal Mode or reception of a dominant bus signal while TxD is recessive.

10. UNDER-VOLTAGE DETECTION

The TJA1041 is able to detect an under-voltage condition on Vcc, Vio and V_{BAT}. Upon detection the TJA1041 is forced into a fail-silent state, which prevents any short-circuit current and thus helps to protect the battery from discharging.

The following table gives a brief overview on the under-voltage detection feature of the TJA1041.

Under-voltage on	Detection condition	Mode change to
Vcc	$Vcc<V_{BAT}-1,4V_{(typ)}$ AND $V_{BAT}<5V$ for longer than under-voltage detection time [1]	Sleep
V_{IO}	$V_{IO}<V_{IO(SLEEP)}$ for longer than under-voltage detection time [1]	Sleep
V_{BAT}	$V_{BAT}<Vcc-1,4V_{(typ)}$; no timeout	Standby

Table 10-1: Supply Under-voltage detection

10.1 Vcc/Vio Under-voltage detection

Upon detection of an Vcc or Vio Under-voltage condition the transceiver is forced autonomously into Sleep Mode overruling the current signal combination on pin "$\overline{STB}$" and pin "EN". As a result the pin "INH" becomes floating, disabling the voltage regulator(s).

An under-voltage condition may occur if the pin "Vcc" and/or pin "Vio" are disconnected or if there is a short circuit from Vcc or Vio to GND e.g. due to a broken capacitor. In case of a short circuit, disabling the voltage regulator prevents flow of high short-circuit current.

The under-voltage condition must hold at least the “under-voltage detection time on Vcc and Vio” before the transceiver is forced into Sleep Mode. This time-out is needed to suppress the under-voltage detection during ramping up of Vcc/Vio, e.g. upon wakeup from Sleep Mode. A wakeup event either received from the bus or the pin “WAKE” will wakeup the transceiver (INH switched on) along with trying to ramp up Vcc and/or Vio again. If there is still an under-voltage condition on Vcc and/or Vio, the transceiver will be forced into Sleep Mode once again.

Notice there is no dedicated signal to inform the microcontroller about a Vcc under-voltage condition at the transceiver. However, the microcontroller can learn from a transceiver under-voltage condition by evaluating the pin “INH”. Whenever a Vcc or Vio under-voltage has been detected by the transceiver, a pull-down resistor would pull the pin “INH” to LOW level.

10.1.1 Application with slow-starting Vcc supply

For a successful start-up of the TJA1041 the Vcc and Vio supply voltage must have ramped up within at least the min. “under-voltage detection time on Vcc or Vio“ [1] after BAT power application or after a wakeup from Sleep Mode (with disabled Vcc supply). In case the INH controlled supply starts too slow,

the TJA1041 may detect a Vcc/Vio under-voltage condition, forcing the transceiver into Sleep Mode. These applications with slow starting supplies would need an extra local wakeup impulse via the pin "WAKE" to get the node alive. Figure 10-1 sketches a possible solution, which is able to generate an extra local wakeup impulse. It includes a capacitor C_{INH} to lengthen the INH "On" signal and a transistor switch at the pin "WAKE, such that a local wakeup pulse can be given from the microcontroller.

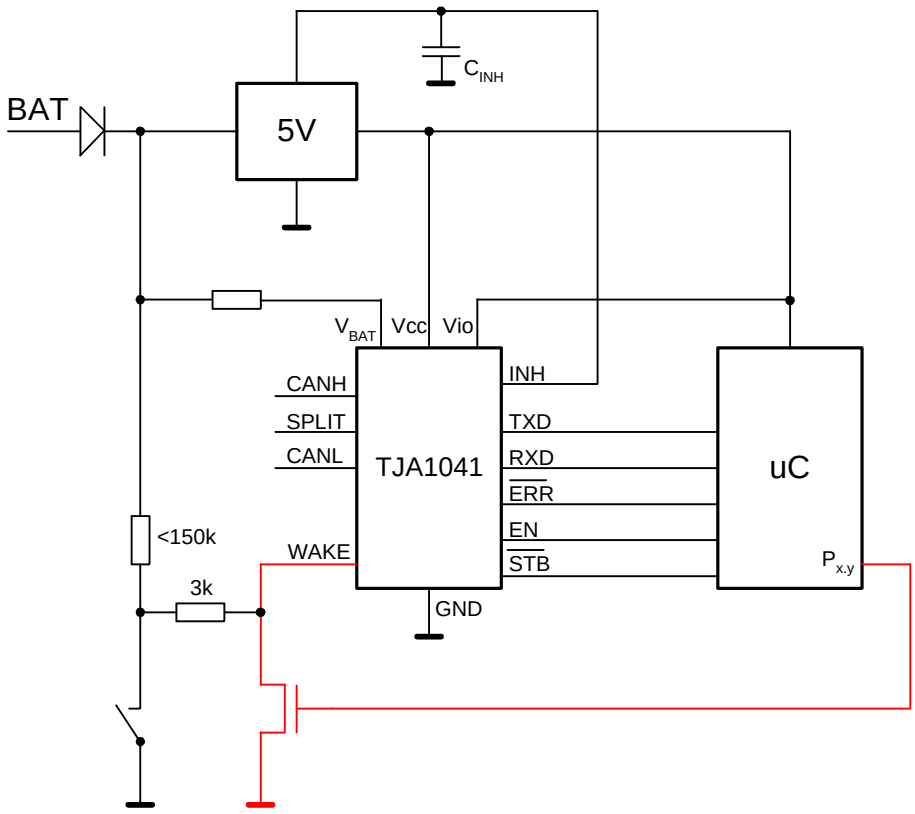


Figure 10-1: Possible application with slow starting Vcc supply

As the wakeup circuit needs some time for recovery ("under-voltage recover time on Vcc and Vio" [1]) after a Vcc/Vio under-voltage has been detected, the extra local wakeup pulse should be given to the transceiver earliest after the max. recovery time from point of the under-voltage detection. The diagram in Figure 10-2 illustrates the timing in more detail.

1. After BAT power application to the TJA1041 the transceiver is initialized, activating INH almost immediately.
2. Because of the large delay in ramping up Vcc, the transceiver may detect a Vcc/Vio under-voltage condition as early as 5ms after battery power application, thus switching off the INH pull-up current and leaving the pin floating.
3. However, due to the INH pulse lengthening of the capacitor C_{INH}, the voltage regulator still keeps active, allowing complete ramp-up of Vcc and initializing the microcontroller.
4. As early as the maximum under-voltage recovery time [1] has expired, the microcontroller can generate a local wakeup to the transceiver. This wakeup should be given first after Vcc has completely ramped

up. As a result the transceiver wakes up from Sleep Mode, entering the mode currently selected at the mode control pins STB and EN.

The value of C_{INH} together with the typical pull-down resistor of the Inhibit input of the voltage regulator determines the RC time constant for discharging the INH capacitance after Vcc under-voltage detection. This RC time constant has to ensure that the voltage on INH keeps well above the Inhibit threshold of the voltage regulator until the local wakeup is given to the transceiver. Notice that due to the extra capacitance there is also an increase of the time constant for charging the INH line. However, this time constant is typically far lower than for discharging (R_{DS} of internal INH switch max. 4450Ω compared to typical pull-down resistors of the Inhibit input of common voltage regulators).

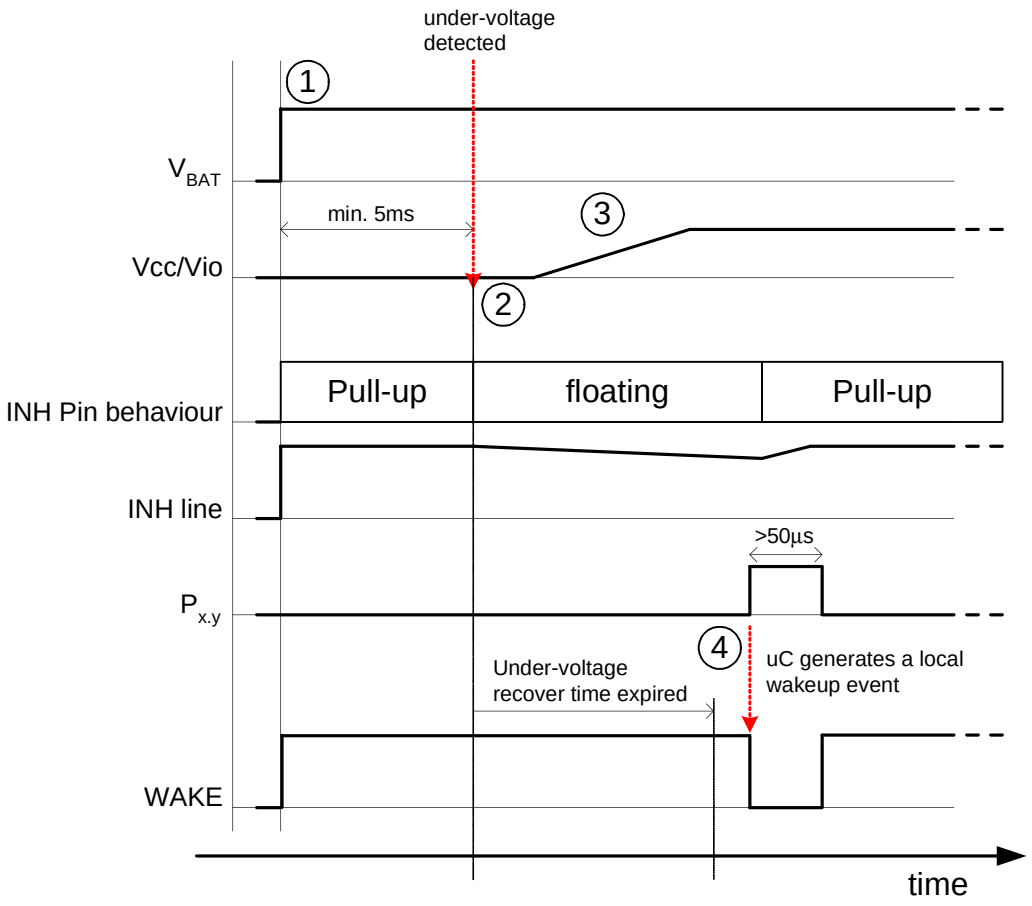


Figure 10-2: Wakeup timing in case of Vcc/Vio undervoltage detection during start-up

10.2 V_{BAT} Under-voltage detection

The TJA1041 monitors the battery supply voltage at the pin "V_{BAT}". If the battery supply voltage falls below the BAT-Under-voltage threshold [1], the transceiver enters autonomously the Standby Mode, overruling the mode control pins "STB" and "EN". An under-voltage condition on the pin "V_{BAT}" may occur for example, if the pin "V_{BAT}" has been disconnected, or temporarily during start of the engine (pulse 4 of ISO7637). The BAT-Under-voltage threshold is related to the Vcc supply voltage. A BAT-Under-

voltage condition is detected only if V_{BAT}< Vcc-1,4$V_{(typ.)}$ and will be taken off again when V_{BAT} crosses the detection threshold $V_{BAT(STANDBY)}$ upwards, leaving mode control to pin $\overline{STB}$ and EN.

In addition, whenever V_{BAT} falls below $V_{BAT(Pwon)}$[1], the PWON flag is set. The microcontroller has access to this flag via the pin "$\overline{ERR}$" when the Pwon/Listen-Only Mode is entered from Sleep, Standby or Go-to Sleep Command Mode. A transition into Normal Mode deletes the PWON flag. In this way the application microcontroller is able to know from a temporary, local battery under-voltage condition.

11. SOFTWARE ISSUES

11.1 Software Flow for Handling Communication Failures

Figure 11-1 suggests a software flow for handling communication failures. Starting from normal operation with the TJA1041 in Normal Mode, the host microcontroller reads the Bus Failure flag at the pin "$\overline{\text{ERR}}$" whenever a communication failure has been reported by an error interrupt of the CAN-controller or by a missing transmit interrupt.

If the Bus Failure flag is set, the communication failure is likely to be caused by a bus failure. After a defined time-out period a new transmission attempt is performed. After a maximum number of transmission attempts have failed, an application appropriate fall-back procedure must be activated. On the other hand, if the Bus Failure flag is not set, the communication failure is likely to be caused by a local failure. In order to check for a local failure condition, the transceiver is forced into Pwon/Listen-Only Mode. If a local failure is signalled (see 9), the application waits for recovery reading periodically the Local Failure flag. If there was no recovery within a defined time-out period, one option can be forcing a transition into Normal Mode with releasing the transmitter. If the failure still exists, again detection will disable the transmitter due to fail-safe reasons.

Another option is to use a fall-back procedure. If reading the Local Failure flag signals that the failure is recovered, the transceiver is put into Normal Mode and normal operation will be ongoing.

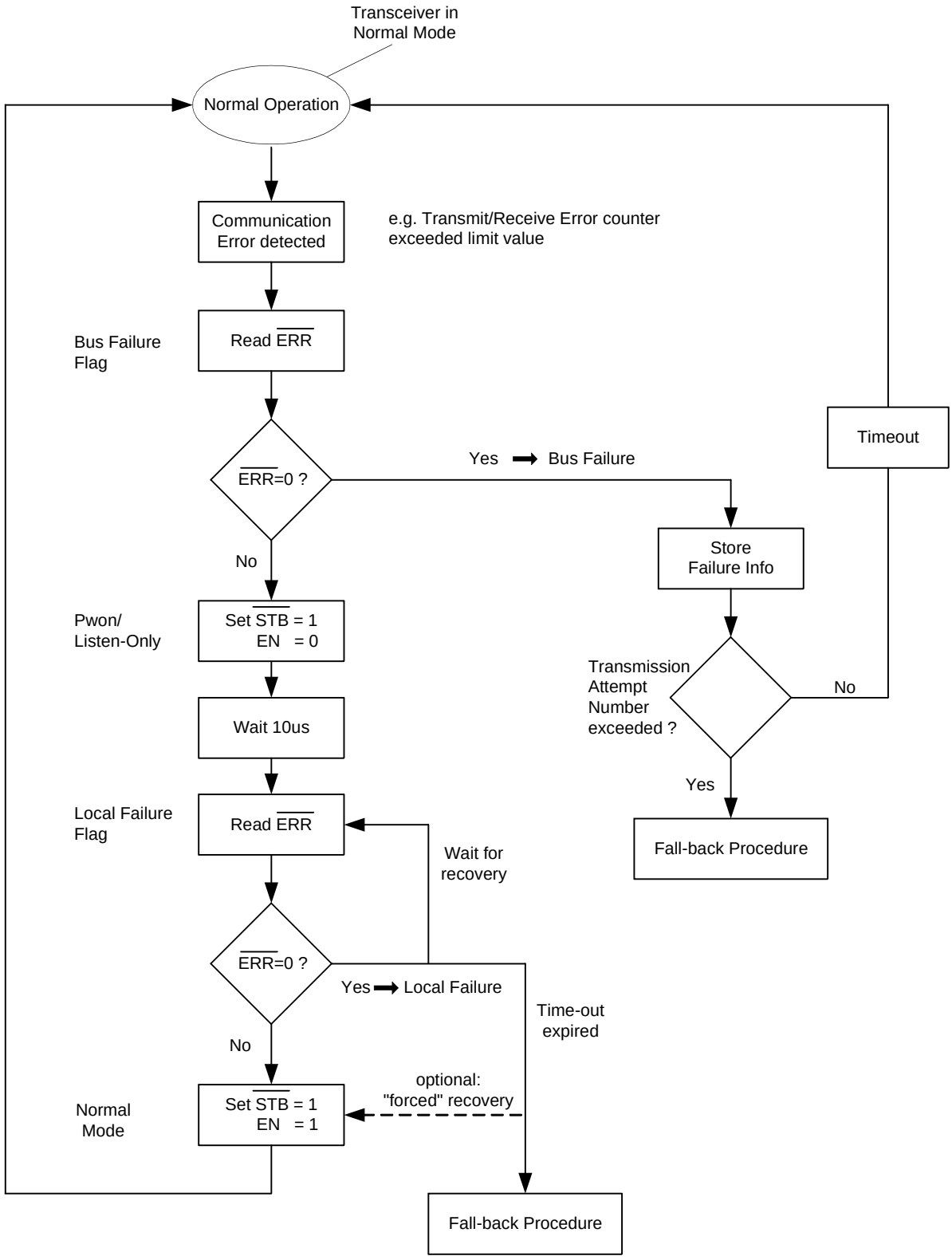


Figure 11-1: Flow diagram for handling communication failures

11.2 Software Flow for an ECU Cold Start

The PWON flag of the TJA1041 indicates to the microcontroller whether a microcontroller cold start was caused by a wakeup from Sleep Mode or by a first battery power application. This information is often needed for the application to initiate some possible calibration procedures upon first battery power application.

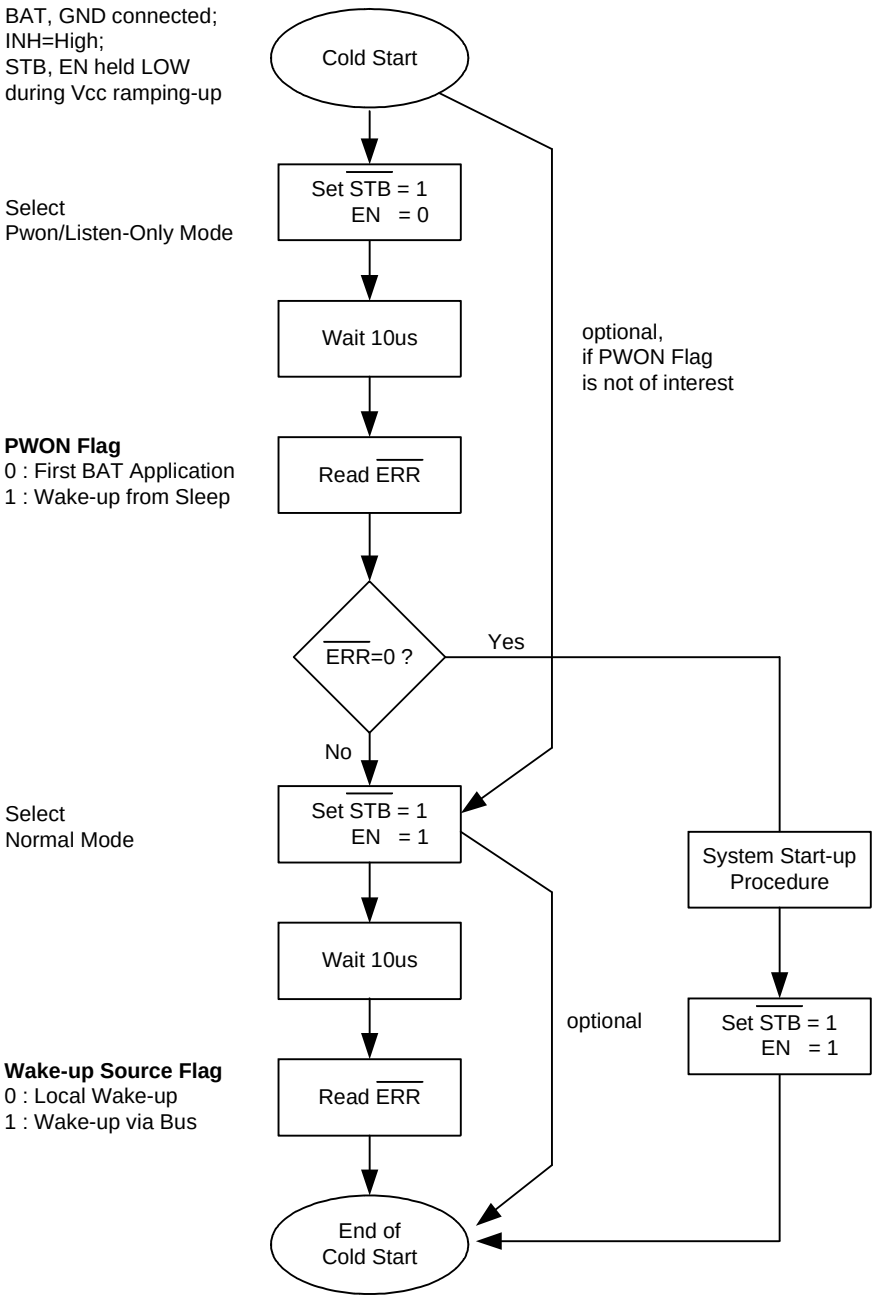


Figure 11-2: Flow diagram for an ECU cold-start

The pin "$\overline{\text{ERR}}$" reflects the PWON flag when entering the Pwon/Listen-Only Mode from Standby, Sleep or Go-to Sleep Command Mode. Moreover, in case of a wakeup from Sleep Mode the TJA1041 provides information on the wakeup source. Entering the Normal Mode the pin "$\overline{\text{ERR}}$" reflects the Wakeup Source flag. A "LOW" signal indicates a local wakeup via the pin "WAKE", whereas a "HIGH" signal indicates a remote wakeup via the bus.

In case battery power is applied for the first time, an internal hardware reset signal is given to the transceiver for initialization. Subsequently the PWON flag is set and the pin "INH" is pulled to V_{BAT}, activating the voltage regulator(s) and ramping up the Vcc supply. Along with Vcc the pins "RXD" and "$\overline{\text{ERR}}$" go to "HIGH" level. With ramping up Vcc the microcontroller comes up. As almost all microcontrollers feature a weak pull-down or floating behaviour at their port pins, the TJA1041 comes up in Standby Mode after first battery power application. This is the starting point for the application program taking over the control now. If the microcontroller comes up with a "HIGH" level at its port pins, the TJA1041 enters immediately the Normal Mode and the PWON flag information is irretrievably lost.

Figure 11-2 suggests a software flow for an ECU cold-start. It considers primarily the issues related to the TJA1041 rather than representing a complete software flow. After the transceiver and microcontroller have performed their initialization, the transceiver is put into Pwon/Listen-Only Mode for reading the PWON flag. If a "LOW" signal is read on the pin "$\overline{\text{ERR}}$", the ECU cold start was initiated by first battery power application and the microcontroller performs the corresponding system start-up procedure. If a "HIGH" signal is read, the cold start was initiated by a wakeup from Sleep Mode. In order to get information on the wakeup source, the Normal Mode is selected. If reading of the pin "$\overline{\text{ERR}}$" yields a "LOW" signal, there was a local wakeup via the pin "WAKE". If reading yields a "HIGH" signal, the wakeup came via the bus. Afterwards the cold start procedure is finished and normal operation is ongoing.

11.3 Software Flow for an ECU Warm-Start

A warm start is performed when the ECU wakes up from standby (low power level 1). Figure 11-3 suggests a software flow for an ECU warm-start. The starting point assumes a TJA1041 transceiver in its Standby Mode and the host microcontroller in a dedicated power-down mode if available. If the transceiver receives a wakeup either via the bus or via the pin "WAKE", the internal wakeup flag is set and signalled at the pin "$\overline{\text{ERR}}$" and "RXD". These signals can be used for wakeup of the microcontroller from its power-down mode. The starting application program can now take control over the transceiver. If the PWON flag is of interest, the microcontroller can force the transceiver into Pwon/Listen-Only Mode for reading the PWON flag. Otherwise the microcontroller can force the transceiver directly into Normal Mode for reading the Wakeup Source flag at the pin "$\overline{\text{ERR}}$".

As the microcontroller remains powered by the Vcc supply, the microcontroller can monitor its port pins for possible wakeup events. Upon detection of a wakeup event the microcontroller can initiate a wakeup by forcing the transceiver directly into Normal Mode. Then reading of the PWON flag or Wakeup Source flag is not necessary.

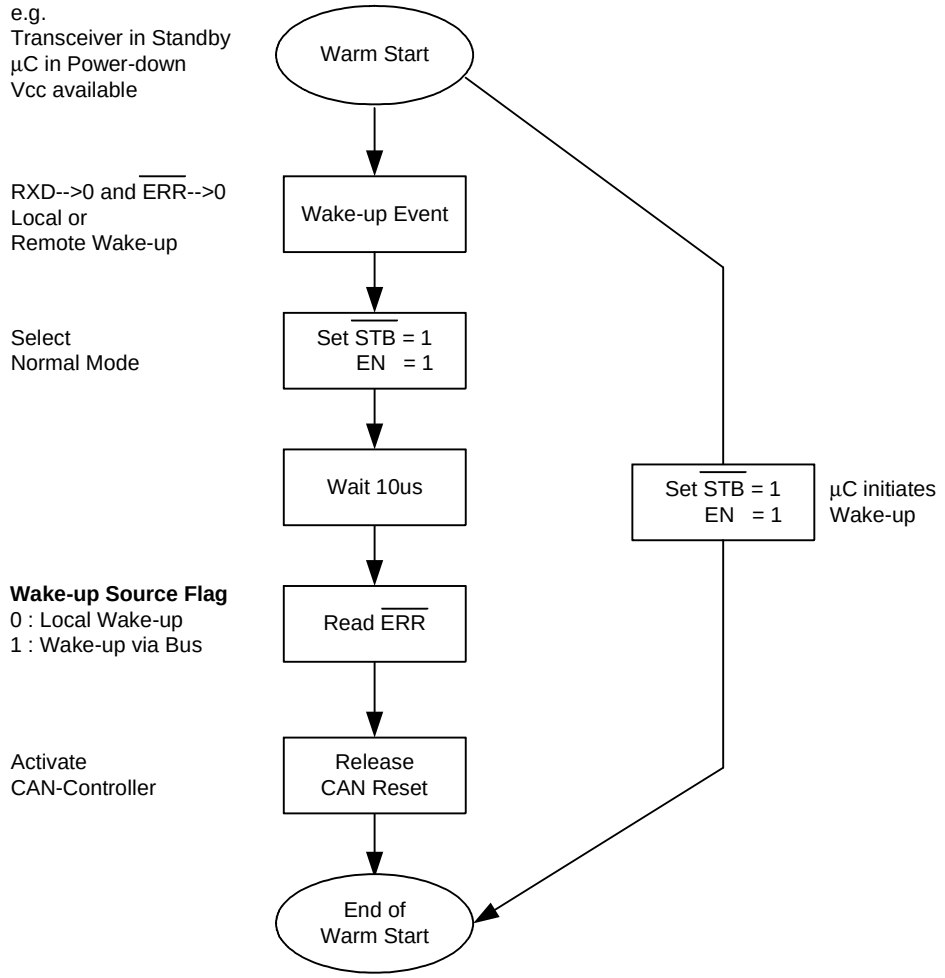


Figure 11-3: Flow diagram for an ECU warm-start

11.4 How to enter Standby Mode (Low Power Level 1)

When the network management decides to put the bus system into Standby, each ECU must receive an appropriate standby command. The flow diagram seen in Figure 11-4 shows the different steps in order to put the TJA1041 into Standby Mode.

Upon receiving a standby command (e.g. using a certain CAN message) the microcontroller has to stop all CAN transmission. In order to ensure that no CAN communication is present on the bus any more, caused by other nodes, the bus must have been recessive for a suitable time before the TJA1041 is put into Standby Mode by selecting $\overline{STB}$=0 and EN=0. If there is no system dependent "waiting period" implemented there would be the risk that a node sends out a last message while another one is already on the way towards Standby Mode. This would cause a wakeup event thus making it impossible to enter a system wide low-power state.

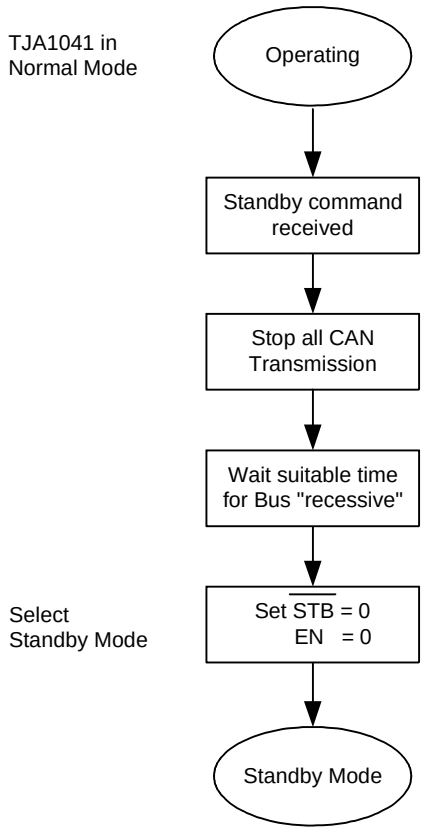


Figure 11-4: Flow diagram for entering Standby Mode

11.5 How to enter Sleep Mode (Low Power Level 2)

The procedure to put an ECU into Sleep as shown in Figure 11-5 is similar to the previous one for entering the Standby Mode. Upon receiving a sleep command the microcontroller has to stop all CAN transmission. In order to ensure that no CAN communication is present on the bus any more, the bus must have been recessive for a suitable time before the TJA1041 is put into Sleep Mode by selecting $\overline{STB}$=0 and EN=1. The difference now is that the microcontroller checks periodically for a wakeup as long as Vcc is not yet down. This is necessary since it might happen that a wakeup event just appears while the Go-to Sleep Command is processed. In this case the INH of the TJA1041 will keep "HIGH" and the Vcc will not drop down. Instead the wakeup request is forwarded to the application via RxD and $\overline{ERR}$ Without this check the microcontroller would assume that a sleep phase follows with disabled Vcc, thus waiting forever for a power-on reset caused by a wakeup which will never happen.

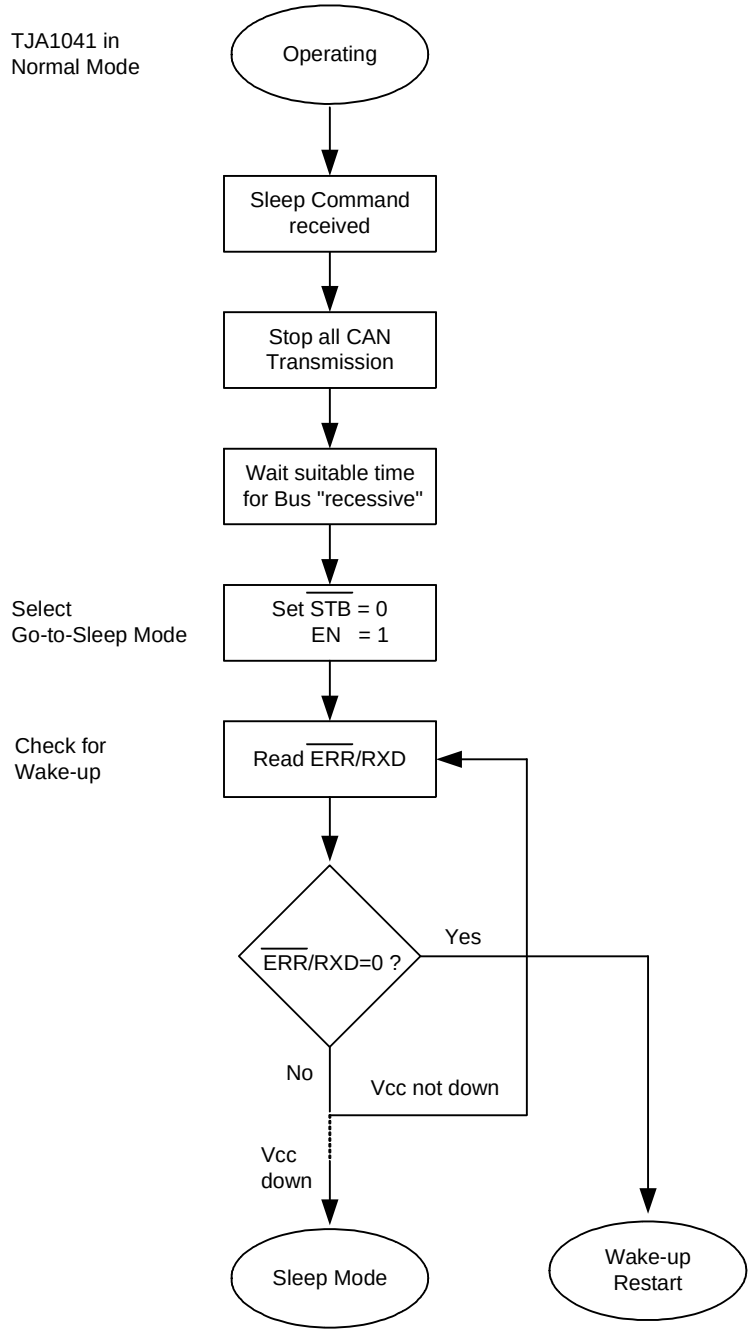


Figure 11-5: Flow diagram for entering Sleep Mode

12. INTEROPERABILITY

Besides the TJA1041, Philips Semiconductors offers the CAN High-Speed Transceiver Products PCA82C250, PCA82C251, TJA1050 and TJA1040. Since all products are compatible with the ISO11898 standard, interoperability with each other is in principle guaranteed. They are able to work together in the same bus network. There are some issues related to different bus biasing behaviour during low-power operation, which shall be considered in this chapter. Table 12-1 shows the bus biasing in the different operation modes as well as in un-powered condition. Whenever there is a difference in the bus biasing, a steady DC common mode current will flow within the system. The common mode input resistance mainly defines the amount of this common mode current. This is shown in Figure 12-1 for a bus in recessive state including TJA1041 and C250 nodes.

Transceiver	Operation mode	Bus Bias
TJA1041	Normal, Pwon/Listen-Only	Vcc/2
	Standby, Sleep, Go-to-Sleep, Unpowered	weak GND
TJA1040	Normal	Vcc/2
	Standby	weak GND
	Unpowered	Floating
TJA1050	Normal, Silent	Vcc/2
	Unpowered	weak GND
C250/C251	Normal, Standby	Vcc/2
	Unpowered	GND

Table 12-1: Bus biasing of Philips Transceivers depending on operation mode

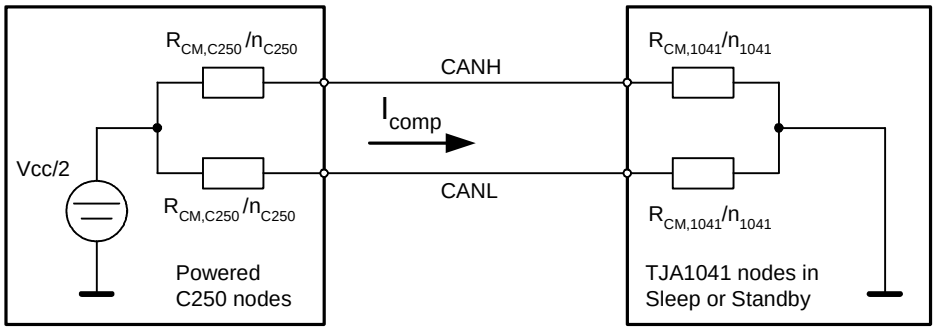


Figure 12-1: Equivalent bus circuit for a mixed system of TJA1041 nodes in Standby/Sleep Mode and powered C250 nodes (in Standby or Normal Mode)

Due to the big common mode input resistance CAN communication is not affected in case parts of the network are still within low-power mode, while other nodes have already started communication. However, degradation of the emission performance is expected.

The following formula allows calculation of the whole biasing compensation current in a mixed system of TJA1041 and C250 nodes.

$$I_{comp,\max} = \frac{Vcc/2}{R_{CM}(C250)/2n_{C250} + R_{CM}(TJA1041)/2n_{TJA1041}}$$

with n_{C250}: number of nodes of powered C250

$n_{TJA1041}$: number of nodes of TJA1041 in Standby/Sleep Mode

$R_{CM}(C250)$ =5k: min. common mode input resistance of C250 at pin CANH/L

$R_{CM}(TJA1041)$ =15k: min. common mode input resistance of TJA1041 at pin CANH/L

Transceiver		TJA1041				
		Normal	Pwon/Listen-Only	Standby	Sleep	Goto-Sleep
TJA1040	Normal	---	---	**X**	**X**	**X**
	Standby	**X**	**X**	---	---	---
	Unpowered	---	---	---	---	---
TJA1050	Normal	---	---	**X**	**X**	**X**
	Silent	---	---	**X**	**X**	**X**
	Unpowered	**X**	**X**	---	---	---
C250/C251	Normal	---	---	**X**	**X**	**X**
	Standby	---	---	**X**	**X**	**X**
	Unpowered	**X**	**X**	---	---	---

Table 12-2: Conditions leading to DC common mode current
X : DC common mode current
---: no DC common mode current

12.1 TJA1041 mixed with C250/C251/TJA1050 nodes

Table 12-2 identifies the conditions leading to different bus biasing and thus DC common mode current. There is some compensation current in case TJA1041 nodes are in Normal (Highspeed) Mode, while other C250/C251/TJA1050 nodes are left un-powered. Moreover, common mode current occurs when TJA1041 nodes are in Standby/Sleep/Go-to-Sleep Mode, while other C250/C251/TJA1050 nodes are kept powered in any operation mode. However, the common mode current is negligible.

12.2 TJA1041 mixed with TJA1040 nodes

Table 12-2 reveals also that in a mixed system of TJA1040 and TJA1041 nodes, it is not expected to have situations of different bus biasing. In the low-power modes both the TJA1040 and TJA1041 show a weak termination to GND. Thus when the bus is in power-down with all nodes either in Standby or Sleep Mode, there will be no DC common mode current. During normal CAN operation, when all nodes are into Normal (Highspeed) or Pwon/Listen-Only Mode for diagnosis features, the bus is collectively biased to Vcc/2. There will be no DC common mode current.

13. REFERENCES

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[4] Data Sheet TJA1054, Fault-tolerant CAN transceiver, Philips Semiconductors, 1999 Febr 11

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[6] Data Sheet PCA82C251, CAN controller interface, Philips Semiconductors, 2000 Jan 13

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[10] IDB-C Physical Layer, Draft Recommended Practice, SAE J2366-1, 2001 May 04

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14. APPENDIX

14.1 Maximum power dissipation within termination resistors

With the help of Figure 14-1 the maximum power dissipation within the termination resistors in case of a bus short circuit is calculated. Assuming a max. short-circuit voltage of 40V on the bus, the max. short-circuit current, which may flow within the TJA1041 while transmitting dominant, is limited to 95mA [1]. As shown in the figure, when one node is transmitting a dominant bit, this short-circuit current is distributed to the two bus terminations, so that each 60Ω termination resistor would dissipate power of

$$P_{dom} = 60\Omega \times (95mA/2)^2 = 135mW$$

The average power dissipation is reduced according to the average recessive/dominant duty cycle on TXD.

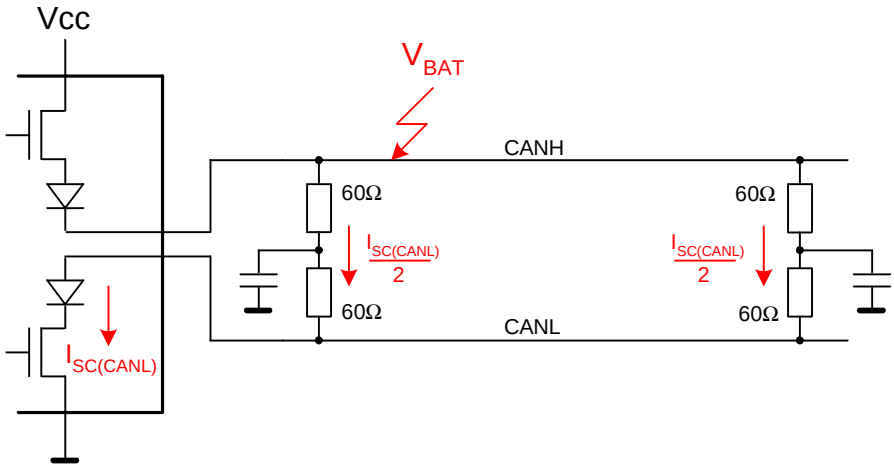

Figure 14-1: Maximum power dissipation within termination resistors

14.2 Vcc Supply Buffering

The TJA1041 needs a BAT-voltage supply and a +5V Vcc supply. The current to drive the bus is delivered by Vcc. The BAT-voltage supply keeps the transceiver alive during Sleep Mode, when the Vcc supply may be off. It maintains the low-power receiver to ensure remote wakeup capability.

In general a capacitor between 47-100nF is recommended being connected between Vcc and GND close to the transceiver. This capacitor buffers the supply voltage during the transition from recessive to dominant, when there is a sharp rise in current demand. An additional bypass capacitor is usually placed at the output of the voltage regulator. Its purpose is to buffer disturbances on the battery line and to buffer extra supply current demand in case of bus failures. To calculate the thermal load of the Vcc voltage regulator the average supply current has to be considered. This can be done in absence and in presence of bus short-circuit conditions.

14.2.1 Vcc Average Supply Current in Absence of Bus Failures

The average supply current depends on the transmit duty cycle. A transmit duty cycle of 50% on pin "TXD" can be assumed as a reasonable value. The maximum average supply current is:

$$I_{CC\_norm\_avg} = 0.5 \cdot \left(I_{CC\_rec\_max} + I_{CC\_dom\_max}\right)$$

Example:
With $I_{CC\_rec\_max}$=13mA and $I_{CC\_dom\_max}$=80mA [1] this results in an average supply current of 47mA.

14.2.2 Vcc Average Supply Current in Presence of Bus Failures

In presence of bus failures the Vcc supply current for the transceiver can increase significantly. It is recommended to dimension the voltage regulator for the worst case of bus failures. Unlike the dominant Vcc supply current I_{CC_dom} the recessive Vcc supply current I_{CC_rec} is not influenced by bus failures. The highest dominant Vcc supply current I_{CC_dom} is flowing in case of a short circuit from CANH to GND. Along with the CANH short circuit output current $I_{SC(CANH)}$ the dominant Vcc supply current I_{CC_dom} calculates to about 123mA. This results in an average supply current of 68mA in worst case of a short circuit from CANH to GND.

14.2.3 Dimensioning the Bypass Capacitor of the Voltage Regulator

As the Vcc voltage provides the internal reference for the receiver input thresholds and bus output voltages, stabilizing the output voltage of the voltage regulator through a bypass capacitor is very important. This bypass capacitor is typically used in combination with the 47nF capacitor close to the transceiver.

The quiescent current delivered from the voltage regulator to the transceiver is determined by the recessive Vcc supply current I_{CC_rec}.

Extra supply current is demanded during dominant transmitting periods. It is calculated by

$$\Delta I_{CC\_ex} = I_{CC\_dom} - I_{CC\_rec}$$

In absence of bus failures the maximum extra supply current is calculated by

$$\Delta I_{CC\_max} = I_{CC\_dom\_max} - I_{CC\_rec\_min}$$

Example:
With $I_{CC\_dom\_max}$=80mA and $I_{CC\_rec\_min}$=7mA the maximum extra supply current calculates to 73mA. Normally, the voltage regulator is strong enough to deliver this extra supply current without significant Vcc voltage drop.

In presence of bus failures the maximum extra supply current may be significantly higher. Considering the worst case of a short circuit from CANH to GND the maximum extra supply current is calculated by

$$\Delta I_{CC\_max\_sc} = I_{CC\_dom\_sc\_max} - I_{CC\_rec\_sc\_min}$$

Example:
With $I_{CC\_dom\_sc\_max}$=123mA and $I_{CC\_rec\_sc\_min}$=7mA the maximum extra supply current calculates to 116mA.

This extra supply current might have to be delivered up to 17 bit times in case of a short circuit from CANH to GND. The reason is that in case of a short circuit from CANH to GND the bus will be clamped to recessive state. The moment the CAN controller starts a transmission, the dominant Start Of Frame bit is not fed back to RXD and thus forces an error frame due to the bit failure condition. The first bit of the error frame again is not reflected at RXD and forces the next error frame (TX Error Counter +8). Latest after 17 bit times, depending on the TX Error Counter Level before starting this transmission, the CAN controller reaches the Error Passive limit (128) and stops sending dominant bits. Now a sequence of

25 recessive bits follows (8 Bit Error Delimiter + 3 Bit Intermission + 8 Bit Suspend Transmission) and the Vcc supply current becomes reduced to the recessive one.

If the voltage regulator is shared by the transceiver and the microcontroller, the Vcc voltage must be maintained during the 17 bit times with increased extra supply current demand. Otherwise the correct operation of the microcontroller can not be guaranteed. Also considering the worst case, one can assume that the complete extra supply current during the 17 bit times has to be buffered by the bypass capacitor. The worst-case bypass capacitor then calculates to

$$C_{Buff} = \frac{\Delta I_{CC\_\max\_sc} \cdot t_{dom\_\max}}{\Delta V_{\max}} = \frac{116mA \cdot 34\mu s}{0{,}2V} \approx 20\mu F ,$$

with $\Delta I_{CC\_\max\_sc} = 116mA$: maximum extra supply current in case of a short circuit from CANH to GND

$t_{dom\_\max} = 34\mu s$: dominant time of 17 bit times at 500kbit/s

$\Delta V_{\max} = 0{,}2V$: maximum allowed Vcc voltage drop

Of course, depending on the regulation capabilities of the used voltage regulator the bypass capacitor may be much smaller. If the transceiver has its own voltage regulator, the Vcc voltage must not necessarily be maintained during the presence of the short circuit from CANH to GND, because in this case the physical layer is completely disturbed and communication is down.